Genesis Microchip Publication

DATA SHEET

gm5020/gm5020-H

Sections in this document and all other related documentation that mention HDCP refer only to the gm5020-H (HDCP-enabled) chip. All other sections apply to both the gm5020-H chip and the gm5020 (non-HDCP) chip.

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Document history

Document	Description	Date
C5020-DAT-01A	Initial Release	June 2000
C5020-DAT-01B	PWM feature documented	June 2000
C5020-DAT-01C	• Pin R1 (HDATA1) does not require pull-up (See Table 5). • FSADDR7 bootstrap functionality corrected. • Figure 59 clarified. • Character attribute word mapping corrections in Sections 0 and 0. • Figure 1 – second EDID EPROM added to clarify the example. • YUV(7:0) incorporate General Purpose Inputs (GPIs). See Section 4.19.1 and Table 4. • Section 4.19.1,General Purpose Inputs and Outputs (GPIO's) added. • RealColor ™ Flesh tone Adjustment feature documented.	July 2000
C5020-DAT-01D	• Revised Preliminary AC Characteristics (5.2)	August 2000
C5020-DAT-01E	• Revised Section 5.1 Preliminary DC Characteristics (Power Figures) • Revised Table 3 (TCLK, XTAL) • Revised Section 4.1 Clocking Options • Added Sections 4.10.10 Input Dithering / Compression and 4.15.2 Output Dithering • Minor clarifications to Sections: 4.2.1; 4.3.4; 4.10.3; 4.19.2 and 4.19.3 and to Figures 1 and 3	August 2000
C5020-DAT-01F	• Revised Table 3 (TCLK, XTAL) • Revised Section 4.1 Clocking Options: add 2.7 K pulldown resistor, TCLK to ground, to maintain correct duty cycle for oscillator • Host Interface Port, HDATA(3:0) pins changed to indicate upper nibble transferred first followed by lower nibble. • Minor clarification to REXT pin description	October 2000
C5020-DAT-01G	• Changed VDD_3.3 and VDD_2.5 MIN and MAX values from TYP +/- 10% to TYP +/- 5% in Table 17. • PWM0 and PWM1 have same functionality 4.19.2.	October 2000
C5020-DAT-01H	• Cosmetic changes to Table 18 - Maximum Speed of Operation • Modified recommended HSYNC input circuit in Figure 6 - Example Signal Terminations • Modified Figure 4 –Clock Generation Options for gm5020 • Added note "(400mV typical hysteresis)" to all Schmitt trigger inputs in Section 3 - Pin List. • Amended I/O column in Table 6 – Display Port Signals	Jan. 2001
C5020-DAT-01I	• In section 1.2 - Features and Analog RGB Input Port - changed SXGA to UXGA. In Analog RGB Input Port, changed frequency to 60Hz. In Ultra-Reliable DVI Receiver, changed frequency to 165MHz. • In section 4.3.4, changed range to "10MHz to 162MHz." • In Table 12 changed input clock to 165MHz. • In Table 16, changed θ_{JC} rating to 7.8. • In Table 17, made extensive changes to parameters and ratings. • In Table 18, included maximum speed of operation (200MHz) for R_CLK Reference Clock. Changed TMDS clock to 165MHz. Changed ADC Clock to 162MHz. Changed F_CLK_Frame Store Clock speed to 144MHz. • In section 14.16.1.1, changed number of words from 3324 to 3594. • In section 6, changed Speed to 162MHz. • In section 3, corrected references to certain signals.	Feb. 2001
C5020-DAT-01J	• In first sentence of section 4.16.1.4, corrected reference to bit setting.	April 2001
C5020-DAT-01K	• In Table 16, changed Input Voltage (5V tolerant inputs) Max to 5.5V	July 2001
C5020-DAT-01L	• In Table 17, included more details about supply current specifications.	July 2001

C5020-DAT-01M	• Updated section 5 with measured values • In Table 13, speed changed to 125 MHz. • Updated section 1 and 1.1 • Updated section 6	
C5020-DAT-01N	• Updated ordering information in section 6. • Inserted HDCP notice on front cover. • Included note in description of pin DDC_SCL in Table 2. • Replaced occurrences of TMDS with DVI.	Nov 2001
C5020-DAT-01O	• Modified description of pins N2 and N3 in Table 2.	Dec 2001
C5020-DAT-01P	• In Figure 11, changed 100 ohm input resistors to 15 ohms. • Added new section 4.8.4 Input Look-up Table. • Updated Figure 1, Figure 3, Figure 8, and Figure 29. • Deleted section about Input Dithering / Compression. • Included new section 4.13.1 DDS. • Added new first sentence to section 4.18. • Modified section 4.18.1.1. • Changed /HFS to /HFSn in Figure 58 and Figure 59. • Modified 2nd paragraph in section 4.19.1. • Case temperature added to Table 16. • Modified Figure 11 and added new explanatory text. • Modified 1st paragraph of section 4.2.1. • Added Figure 9. • Edited text in section 4.5. • In Table 13, speed changed to 120 MHz. • Modified text and graphics in Section 4 substantially.	Jan 2002
C5020-DAT-01Q	• In Table 16, changed values of Case Temperature, Thermal Resistance: (Junction to Ambient), and Thermal Resistance: (Junction to Case). • In Section 4.2.2, added definitions of bits PA, CRO, and RO. • Added note in Section 4.17. • In Table 1, added description of REXT pin. • In Table 2, modified description of REXT pin.	Feb 2002

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1. OVERVIEW

The gm5020 is a graphics processing IC providing high-quality images for LCD monitors and other pixelated displays. It combines a triple ADC, the Genesis Ultra-Reliable DVI™ receiver, a high quality zoom and shrink scaling engine, frame rate conversion, an on-screen display (OSD) controller, a microprocessor and many other functions in a single device. This high level of integration enables simple, flexible, cost-effective solutions featuring fewer required components.

The gm5020 is ideal for dual-interface (analog and digital) LCD monitors up to SXGA resolutions.

1.1 gm5020 System Design Example

Figure 1 below shows a typical dual interface LCD monitor system based on the gm5020. Designs based on the gm5020 have reduced system cost and simplified hardware and firmware design because only a minimal number of components are required in the system. The chip can be used in a variety of systems, ranging from 'single-chassis' solutions for XGA and SXGA monitors with frame store memory and video inputs. In addition, the gm5020 can be used in mid-range SXGA monitors with no frame store memory.

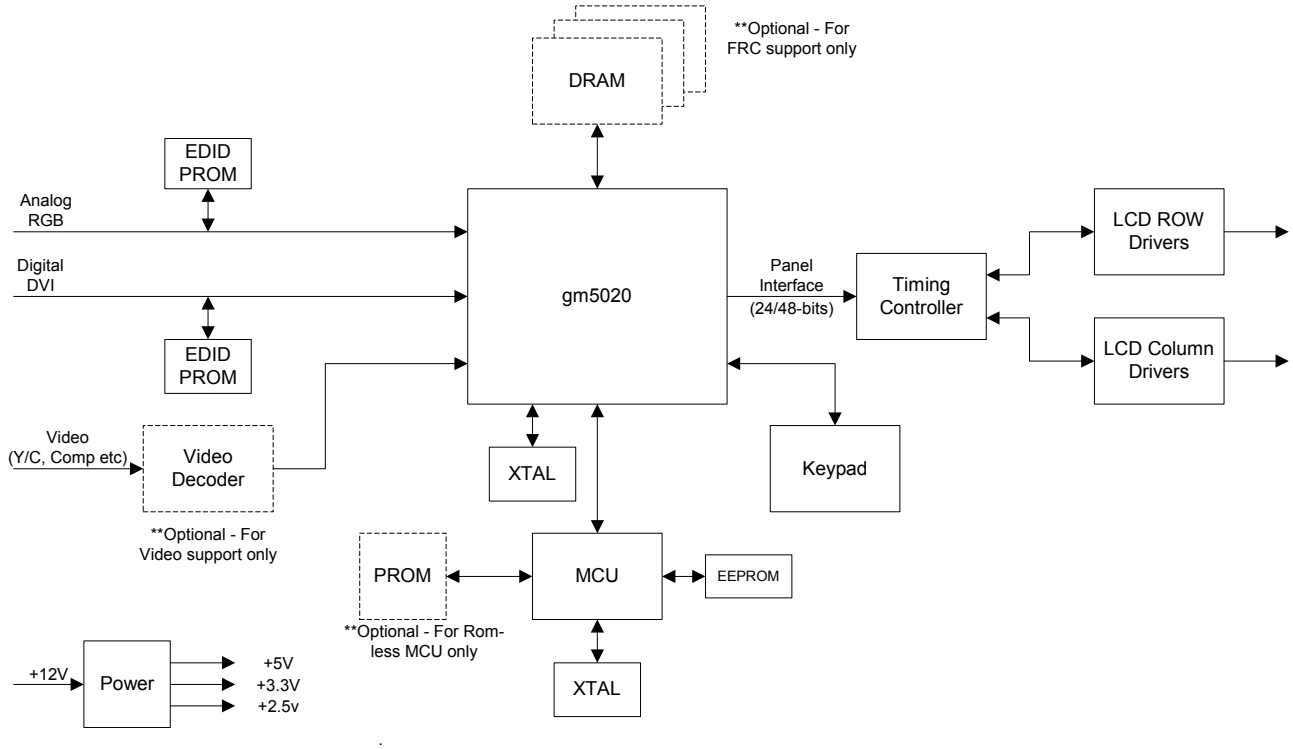


Figure 1. gm5020 System Design Example

1.2 gm5020/gm5020-H Features

FEATURES

- Zoom and shrink scaling (all resolutions from VGA to UXGA)
- Frame rate conversion
- Integrated 8-bit triple-channel ADC / PLL
- Integrated Genesis Ultra-Reliable DVI ™ receiver (DVI 1.0)
- Integrated High-bandwidth Digital Content Protection (HDCP)
- Embedded microcontroller simplifies OSD creation
- On-chip versatile OSD engine
- All system clocks synthesized from a single external crystal
- Programmable gamma correction (CLUT)
- Hue, Saturation, Brightness, Contrast and Gamma controls for RGB and YUV signals
- RealColor™ fleshtone adjustment
- PWM backlight intensity control
- 5 Volt tolerant inputs

- **High-Quality Advanced Scaling**
  - Fully programmable zoom/shrink ratios
  - Independent horizontal / vertical zoom and shrink
  - Variable sharpness control
  - Moiré cancellation

- **Analog RGB Input Port**
  - Supports up to UXGA at 60Hz
  - Support for Sync-on-Green (SOG) and Composite Sync modes

- **Ultra-Reliable DVI Receiver**
  - Single link on-chip DVI receiver
  - Operating up to 165 MHz
  - Direct connect to all DVI-compliant transmitters
  - High-bandwidth Digital Content Protection (HDCP)
  - Enhanced protection of HDCP secret keys

- **Digital Video Port**
  - 8-bit ITU-R BT656 input video
  - Seamless connection to commercially available video capture devices

APPLICATIONS

- Multi-synchronous XGA or SXGA LCD monitors with dual analog/digital interface
- Any fixed-resolution pixelated display device

- **Auto-Configuration / Auto-Detection**
  - Phase and image positioning
  - Input format detection
  - Compatibility with all graphic cards and standard VESA modes

- **Frame Store Interface**
  - Fully-programmable 48 / 32-bit wide data path
  - Optional use of data compression for more flexibility and lower system solution cost
  - Support for up to 143MHz SDRAM or SGRAM

- **On-chip OSD Controller**
  - Bit-mapped OSD capability
  - On-chip RAM for downloadable fonts
  - Horizontal and vertical stretch of OSD images
  - Blinking, transparency and blending

- **Output Format**
  - Single wide up to SXGA 60Hz output
  - Double wide up to SXGA 75Hz output
  - Support for 8 or 6-bit panels (with high-quality dithering)

- **Operating Modes**
  - Frame rate conversion and scaling of images
  - Bypass mode with no filtering and/or frame buffering
  - 1:1 centering
  - De-interlaced zoom
  - Frame Sync and Free Run display synchronization modes

- **Highly Integrated Solution Provides Lowest System Cost**
- **Simplicity of Design Speeds Time to Market**
- **Complete reference design kit available (software and hardware)**

PACKAGE

- 292-pin PBGA

2. PINOUT DIAGRAM

The gm5020 is available in a 292-pin PBGA (Ball Gate Array) package. Figure 2 below provides the ball locations for all signals.

Power and Ground:

DGND	Periphery and Core Digital Ground
DVDD_3.3	Periphery Digital VDD (3.3V supply)
DVDD_2.5	Core Digital VDD (2.5V supply)
PGND	PLL Ground
PLLVDD_3.3	PLL VDD (3.3V supply)
AGND	Analog Ground
AVDD_3.3	Analog VDD (3.3V supply)
AVDD_2.5	Analog VDD (2.5V supply)

Pinout Legend:

DVI
High Frequency Clock
ADC
DDS and PLL

Figure 2. gm5020 Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	N / C	AGND	AGND	AGND	N / C	AVDD_2.5	AVDD_2.5	AVDD_2.5	AVDD_2.5	AVDD_2.5	AVDD_2.5	VCLK	YUV5	YUV2	DBRED7	DBRED4	DBRED1	DBGRN6	DBGRN3	DBGRN2	A
B	AGND	AVDD_3.3	AGND	AGND	N / C	AVDD_3.3	AVDD_3.3	AVDD_3.3	AVDD_3.3	REXT	AVDD_3.3	YUV7	YUV4	YUV1	DBRED6	DBRED3	DBRED0	DBGRN5	DBGRN1	DBGRN0	B
C	BLUE+	BLUE-	AVDD_3.3	AGND	AGND	RXC+	AGND	RX0+	RX1+	RX2+	AGND	YUV6	YUV3	YUV0	DBRED5	DBRED2	DBGRN7	DBGRN4	DBBLU7	DBBLU6	C
D	GREEN-	GREEN+	AVDD_3.3	AGND	AGND	RXC-	AGND	RX0-	RX1-	RX2-	AGND	DVDD_2.5	DVDD_3.3	DVDD_2.5	DVDD_3.3	DVDD_3.3	DVDD_2.5	DBBLU5	DBBLU4	DBBLU3	D
E	RED+	RED-	AVDD_3.3	AGND													DVDD_3.3	DBBLU2	DBBLU1	DBBLU0	E
F	N / C	PLLVDD_3.3	PLLGND	PLLVDD_3.3													DVDD_2.5	DEN	DVS	DHS	F
G	PLLVDD_3.3	PLLGND	PLLVDD_3.3	PLLGND													DVDD_3.3	GPIO6 / DFSYNCn	GPIO7 / DOVL	**DCLK**	G
H	PLLVDD_3.3	PLLGND	PLLGND	**XTAL**				DGND	DGND	DGND	DGND	DGND	DGND				DARED7	DARED6	DARED5	DARED4	H
J	PLLVDD_3.3	PLLGND	PLLVDD_3.3	**TCLK**				DGND	DGND	DGND	DGND	DGND	DGND				DVDD_3.3	DARED3	DARED2	DARED1	J
K	VSYNC	N / C	PLLGND	DVDD_2.5				DGND	DGND	DGND	DGND	DGND	DGND				DVDD_2.5	DARED0	DAGRN7	DAGRN6	K
L	GPIO5	HSYNC	**EXTCLK**	DVDD_3.3				DGND	DGND	DGND	DGND	DGND	DGND				DVDD_3.3	DAGRN3	DAGRN4	DAGRN5	L
M	GPIO4	GPIO3	GPIO2	GPIO1 / PWM1				DGND	DGND	DGND	DGND	DGND	DGND				DVDD_2.5	DAGRN0	DAGRN1	DAGRN2	M
N	GPIO0 / PWM0	DDC_SCL	DDC_SDA	DVDD_2.5				DGND	DGND	DGND	DGND	DGND	DGND				DVDD_3.3	DABLU5	DABLU6	DABLU7	N
P	HCLK / SCL	HFSn / SDA	HDATA3	HDATA2													DVDD_2.5	DABLU2	DABLU3	DABLU4	P
R	HDATA1	HDATA0	IRQn	IRQINn / GPIO8													DVDD_3.3	FSDATA47	DABLU0	DABLU1	R
T	RESETn	DGND	**FSCLK**	DVDD_3.3													DVDD_2.5	FSDATA44	FSDATA45	FSDATA46	T
U	FSCKE	FSWE	FSCAS	DVDD_2.5	DVDD_3.3	DVDD_3.3	DVDD_2.5	DVDD_3.3	DVDD_2.5	DVDD_3.3	DVDD_2.5	DVDD_3.3	DVDD_3.3	DVDD_2.5	DVDD_3.3	DVDD_2.5	DVDD_3.3	FSDATA41	FSDATA42	FSDATA43	U
V	FSRAS	FSADDR13	FSADDR8	FSADDR5	FSADDR2	FSDATA0	FSDATA3	FSDATA6	FSDATA7	FSDATA10	FSDATA15	FSDQM2	FSDATA19	FSDATA22	FSDATA25	FSDATA28	FSDATA31	FSDATA34	FSDATA39	FSDATA40	V
W	FSADDR12	FSADDR10	FSADDR7	FSADDR4	FSADDR1	FSDATA1	FSDATA4	FSDQM0	FSDATA8	FSDATA11	FSDATA14	FSDQM3	FSDATA18	FSDATA21	FSDATA24	FSDATA27	FSDATA30	FSDATA33	FSDATA36	FSDATA38	W
Y	FSADDR11	FSADDR9	FSADDR6	FSADDR3	FSADDR0	FSDATA2	FSDATA5	FSDQM1	FSDATA9	FSDATA12	FSDATA13	FSDATA16	FSDATA17	FSDATA20	FSDATA23	FSDATA26	FSDATA29	FSDATA32	FSDATA35	FSDATA37	Y

3. PIN LIST

I/O Legend: **I** = Input **O** = Output **P** = Power **G**= Ground

Table 1. ADC Signals

Name	I/O	Ball#	Description
REXT	I	B10	External termination resistor. A 1% 1K ohm resistor must be connected from this pin to AVDD_3.3 (3.3V analog power supply). This termination resistor determines current references for both the DVI receiver block and Analog HSYNC Delay block for both DVI and analog configurations.
RED+	I	E1	Positive analog input for Red channel.
RED-	I	E2	Negative analog input for Red channel.
GREEN+	I	D2	Positive analog input for Green channel.
GREEN-	I	D1	Negative analog input for Green channel.
BLUE+	I	C1	Positive analog input for Blue channel.
BLUE-	I	C2	Negative analog input for Blue channel.
HSYNC	I	L2	ADC input horizontal sync or composite sync input. [Input, schmitt trigger (400mV typical hysteresis), 5V-tolerant]
VSYNC	I	K1	ADC input vertical sync. [Input, schmitt trigger (400mV typical hysteresis), 5V-tolerant]

Table 2. DVI Receiver Signals

Name	I/O	Ball#	Description
REXT	I	B10	External termination resistor. A 1% 1K ohm resistor must be connected from this pin to AVDD_3.3 (3.3V analog power supply). This termination resistor determines current references for both the DVI receiver block and Analog HSYNC Delay block for both DVI and analog configurations.
RX2+	I	C10	DVI input channel 2 positive component; RED data and embedded CTL3
RX2-	I	D10	DVI input channel 2 negative component; RED data and embedded CTL3
RX1+	I	C9	DVI input channel 1 positive component; GREEN data
RX1-	I	D9	DVI input channel 1 negative component; GREEN data
RX0+	I	C8	DVI input channel 0 positive component; BLUE data
RX0-	I	D8	DVI input channel 0 negative component; BLUE data
RXC+	I	C6	DVI input clock positive component
RXC-	I	D6	DVI input clock negative component
DDC_SCL	I	N2	For the gm5020-H (HDCP-enabled), this pin is used for DDC Interface for DVI-HDCP communication. This is SCL for slave-only DDC communication. [Input, Schmitt trigger (400mV typical hysteresis), 5V-tolerant] For the gm5020 (non-HDCP), this pin is an unused CMOS input that may be left unconnected. However, it is preferred that this pin be connected to a known logic state.
DDC_SDA	IO	N3	For the gm5020-H (HDCP-enabled), this pin is used for DDC Interface for DVI-HDCP communication. This is SDA for slave-only DDC communication. [Bidirectional, 4mA drive output, Schmitt trigger input (400mV typical hysteresis), 5V-tolerant] For the gm5020 (non-HDCP), this pin is an unused CMOS input that may be left unconnected. However, it is preferred that this pin be connected to a known logic state.

Table 3. RCLK and FCLK PLL Signals

Name	I/O	Ball#	Description
TCLK	O	J4	Feedback connection to crystal. If the reference clock source is a clock oscillator, this pin should be grounded through a 2.7K pulldown resistor.
XTAL	I	H4	Crystal/oscillator input. For crystal, the frequency restrictions are: Min = 14MHz Max = 50MHz. For oscillator, Min = 14 MHz, Max = 24 MHz [3.3V level]

Table 4. Video Input Port Signals

Name	I/O	Ball#	Description
VCLK	I	A12	Input sample clock (27MHz) from video decoder. [Input, 5V-tolerant]
YUV7	I	B12	Input YUV data in ITU-R BT656 format with embedded SAV and EAV.
YUV6		C12	These inputs feature internal pull-downs. Any external pull-ups used on these inputs should not exceed
YUV5		A13	10k ohms. Larger values run the risk of lowering the input high voltage to a value that would create
YUV4		B13	large currents in the input pads.
YUV3		C13	YUV(7:0) incorporate General Purpose Inputs (GPIs) . See Section 4.19.1.
YUV2		A14	[Input, 100KΩ pull-down, 5V-tolerant]
YUV1		B14	
YUV0		C14	

Table 5. Host Controller Interface Signals

Name	I/O	Ball#	Description
HCLK / SCL	I	P1	Host Protocol input clock. HCLK for 6-wire nibble, SCL for 2-wire mode. [Input, schmitt trigger (400mV typical hysteresis), 5V-tolerant]
HFSn / SDA	IO	P2	Host Protocol framing signal for 6-wire nibble mode. Also used as SDA (open drain) signal for 2-wire mode. [Bidirectional, 4mA drive output, Schmitt trigger input (400mV typical hysteresis), 5V-tolerant]
HDATA3	IO	P3	Host Protocol data nibble for 6-wire mode. The upper nibble byte(3:0) is transferred first followed by
HDATA2		P4	lower nibble byte(7:4).
HDATA1		R1	[Bidirectional, 8mA drive output, Schmitt trigger input (400mV typical hysteresis), 5V-tolerant]
HDATA0		R2	
IRQn	O	R3	Interrupt output pin. May be active drive (active low) or open drain. [8mA drive, 5V-tolerant]
IRQINn / GPIO8	IO	R4	Interrupt input to internal 8051 OCM is active low. OCM interrupt#0. This signal is also GPIO8. Always open drain when in GPO mode. [Bidirectional, schmitt trigger input (400mV typical hysteresis), 5V-tolerant, 8mA drive output]
RESETn	I	T1	Hardware Reset signals is active low. [Input, schmitt trigger (400mV typical hysteresis), 5V-tolerant]
EXTCLK	I	L3	External clock. For test purposes only when Display DDS is unused. [Input, 5V-tolerant]
GPIO0 / PWM0	IO	N1	General purpose input/output signal or PWM0. Open drain option via register bit. [Bidirectional, 8mA drive output, Schmitt trigger input (400mV typical hysteresis0, 5V-tolerant]
GPIO1 / PWM1	IO	M4	General purpose input/output signal or PWM1. Open drain option via register bit. [Bidirectional, 8mA drive output, Schmitt trigger input (400mV typical hysteresis0, 5V-tolerant]
GPIO2	IO	M3	General purpose input/output signals. Open drain option via register bit. [Bidirectional, 8mA drive output, Schmitt trigger input (400mV typical hysteresis0, 5V-tolerant]
GPIO3	IO	M2	General purpose input/output signals. Open drain option via register bit. [Bidirectional, 8mA drive output, Schmitt trigger input (400mV typical hysteresis0, 5V-tolerant]
GPIO4	IO	M1	General purpose input/output signals. Open drain option via register bit. [Bidirectional, 8mA drive output, Schmitt trigger input (400mV typical hysteresis0, 5V-tolerant]
GPIO5	IO	L1	General purpose input/output signals. Open drain option via register bit. [Bidirectional, 8mA drive output, Schmitt trigger input (400mV typical hysteresis0, 5V-tolerant]

Table 6. Display Port Signals

Name	I/O	Ball#	Description
GPIO6 / DFSYNCn	IO	G18	GPIO6 by default. Open drain GPO option via register bit. If DFSYNCn is register bit enabled, manual synchronization of display timing causes display timing to jump to its H and V lock load location. [Bidirectional, 8mA drive output, Schmitt trigger input (400mV typical hysteresis0, 5V-tolerant]
GPIO7 / DOVL	IO	G19	GPIO7 by default. Open drain GPO option via register bit. If DOVL is register bit enabled, overlay valid display pixels are indicated by active DOVL. [Bidirectional, 8mA drive output, Schmitt trigger input (400mV typical hysteresis0, 5V-tolerant]
DCLK	O	G20	Display output clock. [Tri-state output, programmable drive 0-24mA, not 5V-tolerant]
DVS	O	F19	Display vertical sync. [default = active high] [Tri-state output, programmable drive 0-24mA, not 5V-tolerant]
DHS	O	F20	Display horizontal sync. [default = active high] [Tri-state output, programmable drive 0-24mA, not 5V-tolerant]
DEN	O	F18	Display Enable frames the output background window. [Tri-state output, programmable drive 0-24mA, not 5V-tolerant]
DARED7 DARED6 DARED5 DARED4 DARED3 DARED2 DARED1 DARED0	O	H17 H18 H19 H20 J18 J19 J20 K18	Display output red data (even or left pixel). [Tri-state output, programmable drive 0-24mA, not 5V-tolerant]
DAGRN7 DAGRN6 DAGRN5 DAGRN4 DAGRN3 DAGRN2 DAGRN1 DAGRN0	O	K19 K20 L20 L19 L18 M20 M19 M18	Display output green data (even or left pixel). [Tri-state output, programmable drive 0-24mA, not 5V-tolerant]
DABLU7 DABLU6 DABLU5 DABLU4 DABLU3 DABLU2 DABLU1 DABLU0	O	N20 N19 N18 P20 P19 P18 R20 R19	Display output blue data (even or left pixel). [Tri-state output, programmable drive 0-24mA, not 5V-tolerant]
DBRED7 DBRED6 DBRED5 DBRED4 DBRED3 DBRED2 DBRED1 DBRED0	O	A15 B15 C15 A16 B16 C16 A17 B17	Display output red data (odd or right pixel). [Tri-state output, programmable drive 0-24mA, not 5V-tolerant]
DBGRN7 DBGRN6 DBGRN5 DBGRN4	O	C17 A18 B18 C18	Display output green data (odd or right pixel). [Tri-state output, programmable drive 0-24mA, not 5V-tolerant]

Name	I/O	Ball#	Description
DBGRN3		A19	
DBGRN2		A20	
DBGRN1		B19	
DBGRN0		B20	
DBBLU7	O	C19	Display output blue data (odd or right pixel).
DBBLU6		C20	[Tri-state output, programmable drive 0-24mA, not 5V-tolerant]
DBBLU5		D18	
DBBLU4		D19	
DBBLU3		D20	
DBBLU2		E18	
DBBLU1		E19	
DBBLU0		E20	

Table 7. Frame Store Interface Signals

Name	I/O	Ball#	Description
FSCLK	O	T3	SDRAM clock. This signal is rising edge active. [Tri-state output, Programmable Drive 0-24mA, not 5V-tolerant]
FSCKE	O	U1	SDRAM clock enable. This signal is active high. [Tri-state output, 8mA drive, 5V-tolerant]
FSRAS	O	V1	SDRAM row address strobe. This signal is active low [Tri-state output, 8mA drive, 5V-tolerant]
FSCAS	O	U3	SDRAM column address strobe. This signal is active low. [Tri-state output, 8mA drive, 5V-tolerant]
FSWE	O	U2	SDRAM write enable. This signal is active low. [Tri-state output, 8mA drive, 5V-tolerant]
FSDQM3 FSDQM2 FSDQM1 FSDQM0	O	W12 V12 Y8 W8	SDRAM data masks. Each bit enables one of four SDRAM byte “lanes”. This allows host OSD access to the SDRAM to be byte oriented. This signal is active high. Bit 0 enables FSDATA(7:0). Bit 1 enables FSDATA(15:8). Bit 2 enables FSDATA(23:16). Bit 3 enables FSDATA(31:24). [Tri-state output, 8mA drive, 5V-tolerant]
FSADDR13 FSADDR12 FSADDR11 FSADDR10 FSADDR9 FSADDR8 FSADDR7 FSADDR6 FSADDR5 FSADDR4 FSADDR3 FSADDR2 FSADDR1 FSADDR0	IO	V2 W1 Y1 W2 Y2 V3 W3 Y3 V4 W4 Y4 V5 W5 Y5	SDRAM multiplexed address bus. FSADDR[13:0] are used for bootstrapping configuration. See Section 4.17. [Bidirectional, 8mA drive output, 5V-tolerant]

FSDATA47	IO	R18	SDRAM data bus. Optionally programmable to 48 or 32 bits wide. Default is 32 bits wide.
FSDATA46		T20	[Bidirectional, 8mA drive output, 100KΩ pull-down, 5V-tolerant]
FSDATA45		T19	
FSDATA44		T18	
FSDATA43		U20	
FSDATA42		U19	
FSDATA41		U18	
FSDATA40		V20	
FSDATA39		V19	
FSDATA38		W20	
FSDATA37		Y20	
FSDATA36		W19	
FSDATA35		Y19	
FSDATA34		V18	
FSDATA33		W18	
FSDATA32		Y18	
FSDATA31		V17	
FSDATA30		W17	
FSDATA29		Y17	
FSDATA28		V16	
FSDATA27		W16	
FSDATA26		Y16	
FSDATA25		V15	
FSDATA24		W15	
FSDATA23		Y15	
FSDATA22		V14	
FSDATA21		W14	
FSDATA20		Y14	
FSDATA19		V13	
FSDATA18		W13	
FSDATA17		Y13	
FSDATA16		Y12	
FSDATA15		V11	
FSDATA14		W11	
FSDATA13		Y11	
FSDATA12		Y10	
FSDATA11		W10	
FSDATA10		V10	
FSDATA9		Y9	
FSDATA8		W9	
FSDATA7		V9	
FSDATA6		V8	
FSDATA5		Y7	
FSDATA4		W7	
FSDATA3		V7	
FSDATA2		Y6	
FSDATA1		W6	
FSDATA0		V6	

Table 8. Power and Ground Signals

Group Name	I/O	Ball #	Description
PLLGND	G	F3, G2, G4, H2, H3, J2, K3	Analog PLL / DDS Ground
PLLVDD_3.3	P	F2, F4, G1, G3, H1, J1, J3	Analog PLL / DDS 3.3VDC Bypass to PLLGND (0.1uF)
AGND	G	A2, A3, A4, B1, B3, B4, C4, C5, C7, C11, D4, D5, D7, D11, E4	Analog Ground
AVDD_2.5	P	A6, A7, A8, A9, A10, A11	Analog 2.5VDC Supply Bypass to AGND (0.1uF)
AVDD_3.3	P	B2, B6, B7, B8, B9, B11, C3, D3, E3	Analog 3.3VDC Supply Bypass to AGND (0.1uF)
DGND	G	H8, H9, H10, H11, H12, H13, J8, J9, J10, J11, J12, J13, K8, K9, K10, K11, K12, K13, L8, L9, L10, L11, L12, L13, M8, M9, M10, M11, M12, M13, N8, N9, N10, N11, N12, N13, T2	Digital Ground (Periphery and Core Logic)
DVDD_2.5	P	D17, D14, D12, F17, K4, K17, M17, N4, P17, T17, U4, U7, U9, U11, U14, U16	Digital VDD, 2.5VDC (Core Logic. Bypass to DGND, 0.1uF)
DVDD_3.3	P	D16, D15, D13, E17, G17, J17, L4, L17, N17, R17, T4, U5, U6, U8, U10, U12, U13, U15, U17	Digital VDD, 3.3VDC (I/O pins. Bypass to DGND, 0.1uF)

Table 9. No Connects

Group Name	I/O	Ball #	Description
N / C	-	A1, A5, B5, F1, K2	No Connect. Leave these pins floating.

4. FUNCTIONAL DESCRIPTION

A functional block diagram is illustrated below. Each of the functional units shown is described in the following sections.

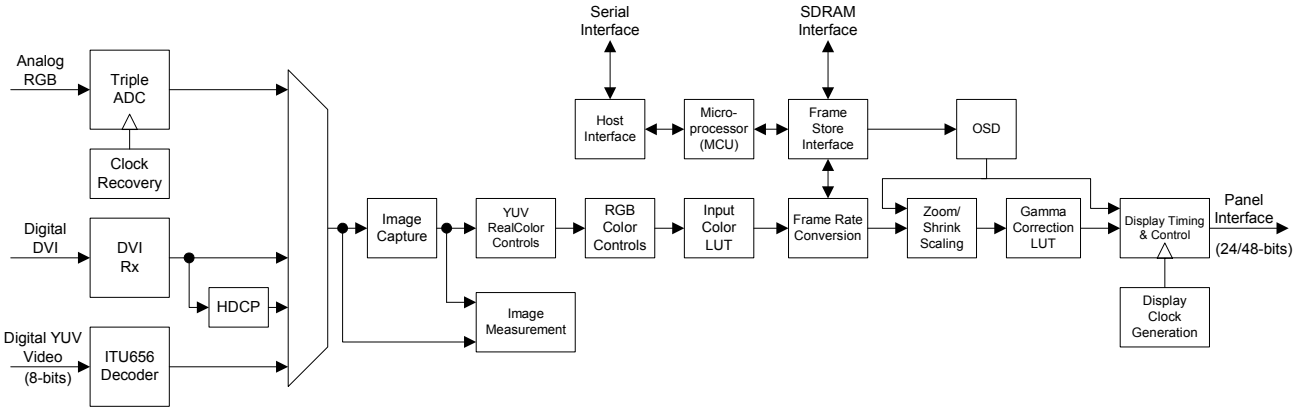


Figure 3. gm5020 Functional Block Diagram

4.1 Clocking Options

The gm5020 features four clock inputs:

1) Timing Clock (TCLK). This is a required clock used as a reference frequency source for the gm5020. Additional clocks are synthesized internally using this reference. TCLK may be connected to a crystal resonator or external oscillator and is further described below.

2) DVI Differential Input Clock (RC+ and RC-). Provided by the external DVI interface.

3) Video Clock (VCLK) input pin. Provided by the external video decoder.

4) Host Interface Transfer Clock (HCLK for 6-Wire nibble; SCL for 2-wire serial). Provided by the external micro controller (MCU).

4.1.1 TCLK Requirements

The TCLK may be generated using either a crystal resonator circuit (recommended) or an external clock oscillator. The TCLK frequency should range between 14 and 50 MHz, though 24 MHz is preferred.

If TCLK is derived from a crystal resonator, an internal oscillator circuit generates a very low jitter and low harmonic clock within the gm5020. The crystal should be connected between the XTAL and TCLK pins and utilize appropriately sized loading capacitors. C_{L1} and C_{L2} are terminated to AVDD_33 to increase the power supply rejection ratio. This is shown in the diagram below.

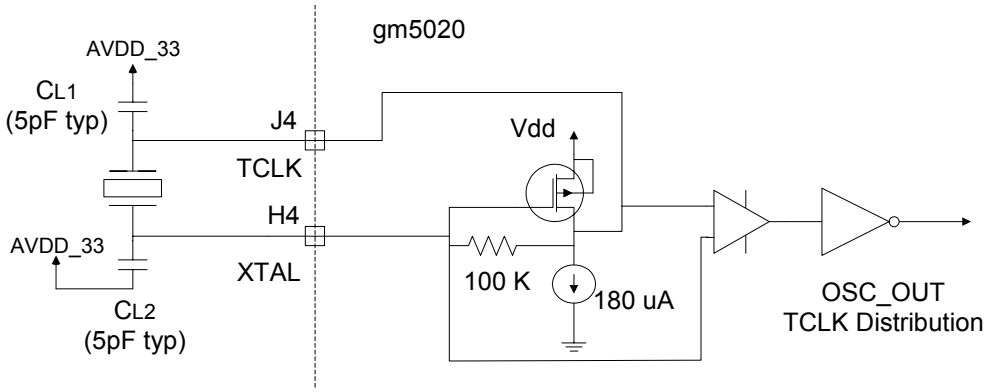


Figure 4. TCLK connection (with Crystal Resonator)

The size of C_{L1} and C_{L2} are determined from the crystal manufacturer's specification and the parasitic capacitance of the gm5020 and PCB traces. To avoid start up problems with the internal oscillator, the C_{LOAD} parameter specified by the crystal manufacturer should not be exceeded. C_{LOAD} includes C_{L1}, C_{L2} as well as the parasitic capacitances. Specifically, these include the

internal shunt capacitance between XTAL and TCLK (C_{SHUNT}), the PCB board capacitance (C_{PCB}) and internal pin, pad and ESD protection capacitance. ($C_{PIN,}$ C_{PAD}, C_{ESD})

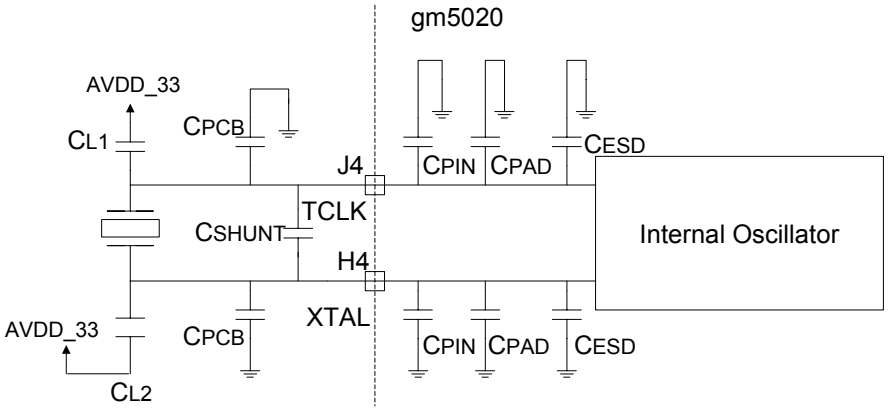


Figure 5. TCLK parasitic capacitances

$C_{LOAD} = C_{SHUNT} + ((C_{LOAD1} * C_{LOAD2}) / (C_{LOAD1} + C_{LOAD2}))$

Where

$C_{LOAD1} = C_{L1} + C_{PCB} + C_{PIN} + C_{PAD} + C_{ESD}$

$C_{LOAD2} = C_{LOAD1}$ (i.e., $C_{L2} = C_{L1}$)

The following values can be used for the gm5020:

C_{SHUNT} ~ 9pF

C_{ESD} ~ 5.3 pF

C_{PAD} ~ 1 pF

C_{PIN} ~ 1.1 pF

C_{PCB} is layout dependent (usually 2 to 10 pF)

In addition to the above requirement, the crystal should be a parallel resonate cut and the equivalent series resistance must be less than 90 ohms. If the equivalent series resistance is greater than 90 ohms, the oscillator may not start. In this case, the internal oscillator gain may be increased by adding a 2.2 kohm resistor from TCLK pin to ground.

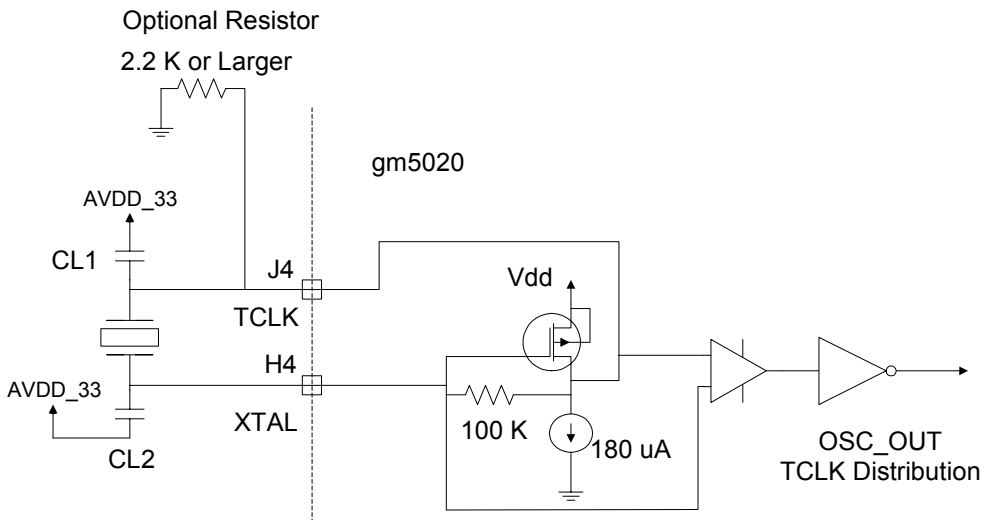


Figure 6. TCLK connection (with Optional Resistor)

If TCLK is derived from an external oscillator, the applied signal should be made to the XTAL pin. A 2.7 kohm resistor from the TCLK pin to ground provides additional bias to keep the clock symmetrical.

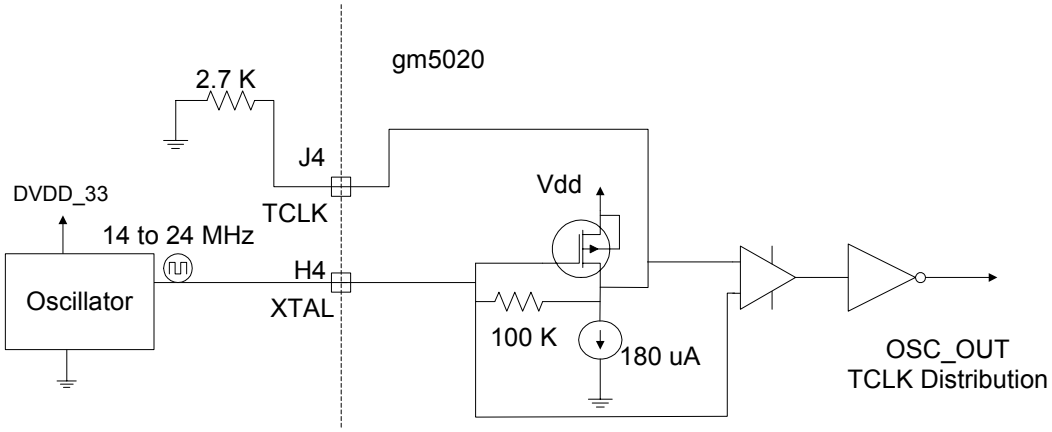
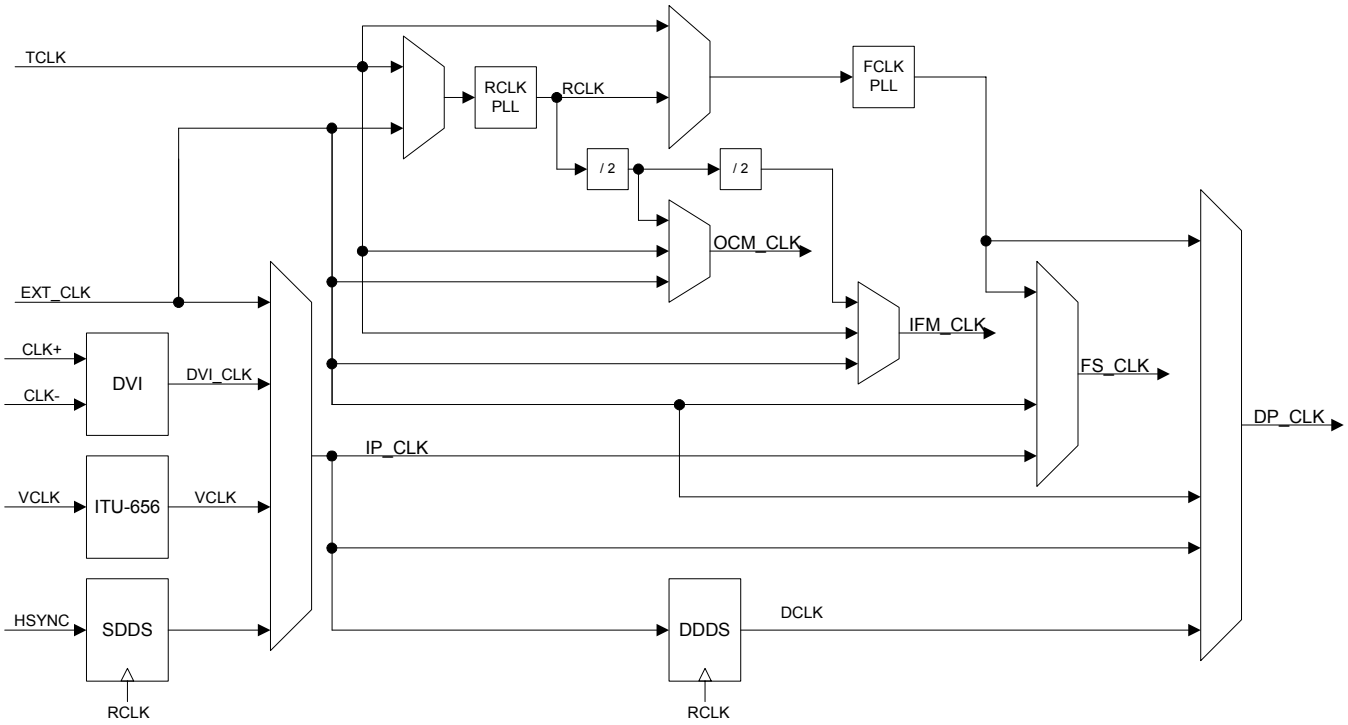


Figure 7. TCLK connection (with Oscillator)

4.1.2 Synthesized Clocks

The gm5020 synthesizes all additional clocks internally: Clock inputs to the DDDS and FCLK PLL (as shown in the figure below) are selected via a host interface register.

Note that even when the system is designed without a frame store interface, an internally synthesized frame store clock (FS_CLK) is required to clock data in and out of internal FIFOs.



Notes: RCLK nominally ~200 MHz;
SDDS=Source Direct Digital Synthesis
DDDS = Display Direct Digital Synthesis

Figure 8. Internal Clock Sources

4.2 Hardware and Software Resets

4.2.1 Hardware Reset

Hardware Reset is performed by holding the RESETn pin low for a minimum of 1µs after the supply voltages are stable, as illustrated in Figure 9. A TCLK input (see Clock Options above) must be applied during and after the reset. When the reset period is complete and RESETn is de-asserted, the gm5020 follows an internal power up sequence:

1. All registers of all types are reset to their default state
2. Each clock domain is internally reset. The reset period remains asserted for 64 local clock domain cycles following the de-assertion of RESETn.
3. The OCM_CLK domain operates at the T_CLK frequency during this period.
4. The RCLK PLL internally produces a 10x output clock (from TCLK reference).
5. The IC will wait for RCLK PLL to Lock and then switch the OCM_CLK to the bootstrap selected clock.
6. The OCM will begin operating if bootstrapped to start operation after Hardware Reset, otherwise it remains in reset until register enabled.

4.2.2 Software Reset

Software Reset is performed by programming the HOST_CONTROL register bit SOFT_RESET = ’0’. The SOFT_RESET bit will self clear to ‘0’ upon completion of reset. The following internal operations occur with software reset:

1. All active and status registers (i.e. the active part of PA bits, and CRO and RO bits unless otherwise indicated) are reset to their default state. Pending and read/write registers remain unaffected. PA, CRO, and RO bits are defined below:

   PA **Pending and active read write bit.** Two registers are used to store these bits: a pending register and an active register. The pending register is transferred to the active register on an update event. The clock domain for each PA register is indicated within square brackets ‘[ ]’ in the register listing (e.g. the active part of register 0x1B6 DISPLAY_CONTROL PA [DP_CLK] will be updated on an update event synchronized to the rising edge of DP_CLK.)

   Only the active register contents affect chip functionality. The active register bits are cleared to ‘0’, unless otherwise specified, by software or hardware reset. The pending register bits are only cleared by a hardware reset, and may be overwritten at any time.

   CRO **Clearable read only status bit.** These are read only registers that may be cleared to ‘0’ when overwritten with a ‘1’. This type is most commonly used for interrupt status registers. These are cleared to ‘0’ by both software and hardware reset.

   RO **Read only status bit.** These are read only registers. No effect to the chip will occur if an attempt is made to write to these bits

2. Each clock domain in the gm5020 is internally reset for 64 local clock domain cycles, before returning to normal operation.

   Software Reset will NOT reset the analog components of the RCLK PLL, FCLK PLL, SDDS, DDDS, DVI, or ADC blocks. Software reset does not affect the IFM.

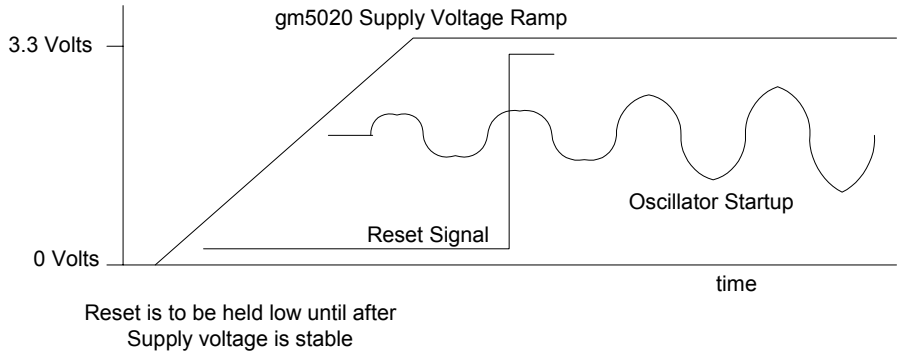


Figure 9. Hardware Reset

4.3 Analog to Digital Converter

The gm5020 chip has three ADC's (analog-to-digital converters), one for each color (red, green, and blue).

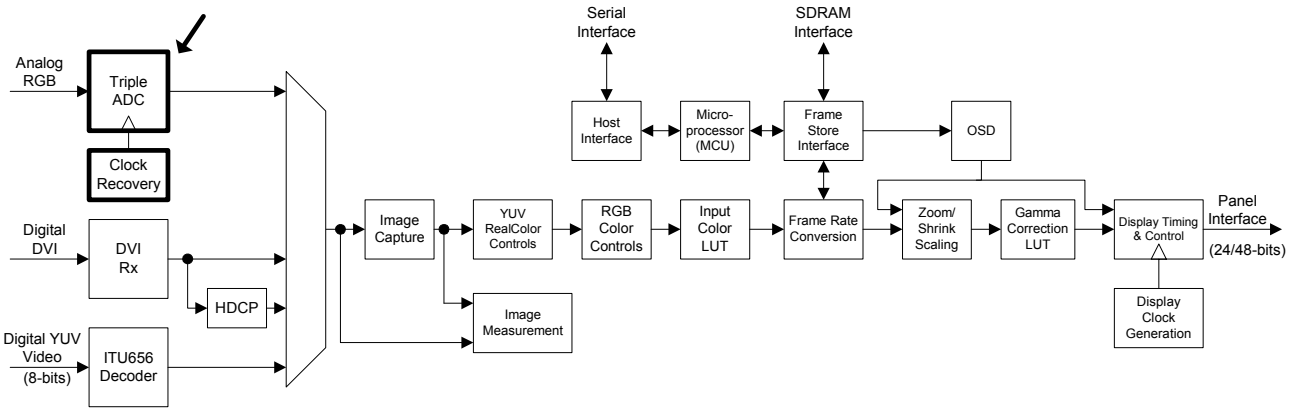


Figure 10. ADC Block

4.3.1 Pin Connection

The RGB signals are connected to the gm5020 as described below:

Table 10. Pin Connection for RGB Input with HSYNC/VSYNC

Pin Name	ADC Signal Name
Red+	Red
Red-	Terminate as illustrated in Figure 11
Green+	Green. When using Sync-On-Green, this signal also carries the sync pulse
Green-	Terminate as illustrated in Figure 11
Blue+	Blue
Blue-	Terminate as illustrated in Figure 11
HSYNC/CS	Horizontal Sync (Terminate as illustrated in Figure 11) or Composite Sync
VSYNC	Vertical Sync (Terminate as with HSYNC illustrated in Figure 11)

The gm5020 HSync and VSync input pins contain Schmitt trigger with typical hysteresis of 350 mV. It is possible to encounter some combinations of video sources, cable, and PCB layout that will exhibit ringing or glitching at the sync signal edges. In severe cases, the glitching may exceed the internal hysteresis provided and cause "false" triggering within the chip. Using external Schmitt triggers can help eliminate this problem. Figure 11 shows the use of external Schmitt triggers on the Hsync and VSync input pins. A device such as the 74AC14 provides typical hysteresis of 1 volt. Using two Schmitt triggers in series provides a buffered sync signal with very little distortion.

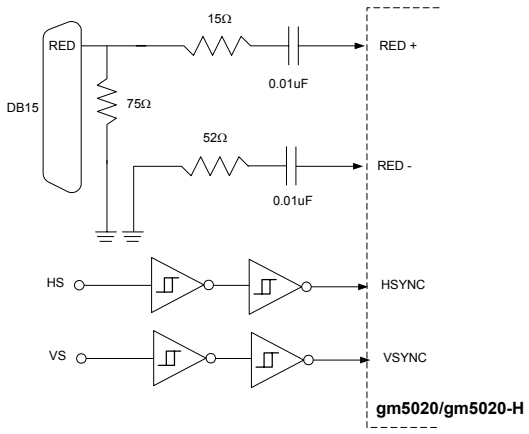


Figure 11. Example Signal Terminations

The negative inputs (eg. RED-) are terminated with an additional 37.5 ohms relative to the positve inputs. This creates a balanced situation for the input amplifier (the positive channel has two 75 ohm terminations in parallel). Please note that it is very important to follow the recommended layout guidelines for the circuit shown above. These are described in "gm5020/5060 System Layout Guidelines" document number C5020-APN-01D.

4.3.2 ADC Characteristics

The table below summarizes the characteristics of the ADC:

Table 11. ADC Characteristics

	MIN	TYP	MAX	NOTE
RGB Track & Hold Amplifiers				
Bandwidth		290MHz		
Settling Time to 1 %		5. 2ns		Full Scale Input = 0.75V, BW=290MHz (*)
Full Scale Adjust Range @ RGB Inputs	0.55 V		0.90 V	
Full Scale Adjust Sensitivity		+/- 1 LSB		Measured @ ADC Output (**)
Zero Scale Adjust Range				AC coupling is used to remove the offset.
Zero Scale Adjust Sensitivity		+/- 1 LSB		Measured @ ADC Output
ADC + RGB Track & Hold Amplifiers				
Sampling Frequency (fs)	20 MHz		162 MHz	
Differential Non-Linearity (DNL)		+/-0.5 LSB		fs = 135MHz
Integral Non-Linearity (INL)		+/- 1.5 LSB		fs = 135 MHz
Channel to Channel Matching		+/- 0.5 LSB		
Effective Number of Bits (ENOB)		7 Bits		fin = 1 MHz, fs = 80 MHz Vin= -1 dB below full scale = 0.75V

(*) Guaranteed by design (**) Independent of full scale RGB input

The gm5020 ADC has a built in clamp circuit. By inserting series capacitors (10 nF), the DC offset of the video source can be removed. The clamp position and width are programmable.

4.3.3 Sync. Signal Support

The gm5020 chip supports digital separate sync (HSYNC/VSYNC), digital composite sync, and analog composite sync (also known as sync-on-green, or SOG). All sync types are supported without the need for external sync separation / extraction circuits.

Digital Composite Sync

In general, the gm5020 supports standard implementations of both OR/AND type and XOR type composite sync signals. Sync status information is available through host registers to interpret the signal type and program its support.

- OR/AND type: No CSYNC pulses toggle during the vertical sync period
- XOR type: CSYNC polarity changes during the vertical sync period

The following waveforms, showing specific implementations of CSYNC, are supported by the Genesis reference firmware. Channel 2 shows the CSYNC waveform while Channel 4 shows the equivalent VSYNC interval. Other variations may or may not be supported and the user should contact Genesis Microchip.

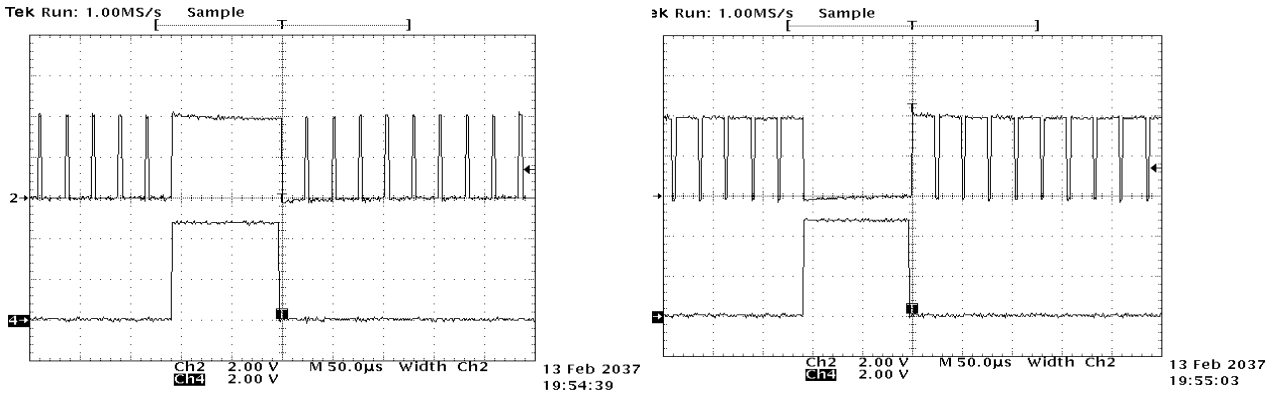


Figure 12. Positive and negative polarity OR-type CSYNC

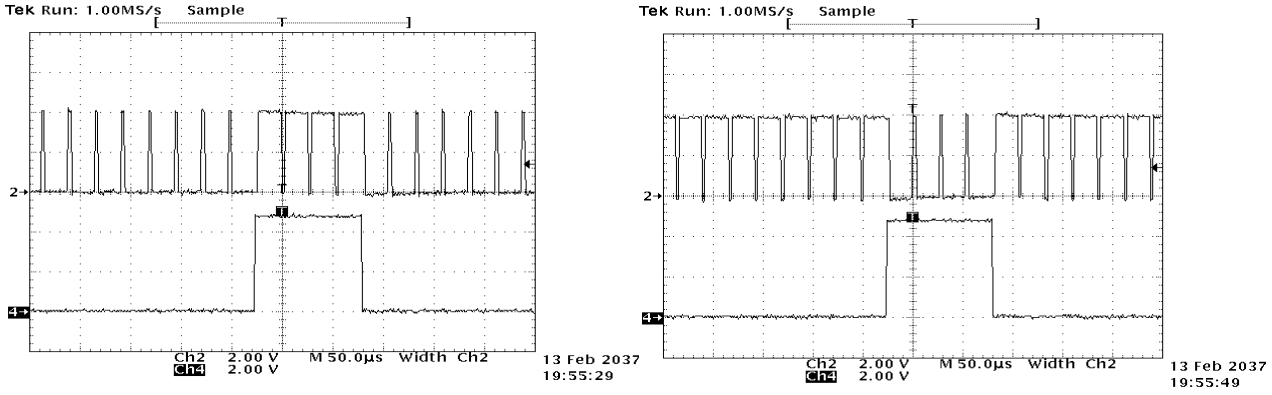


Figure 13. Positive and negative polarity XOR-type CSYNC

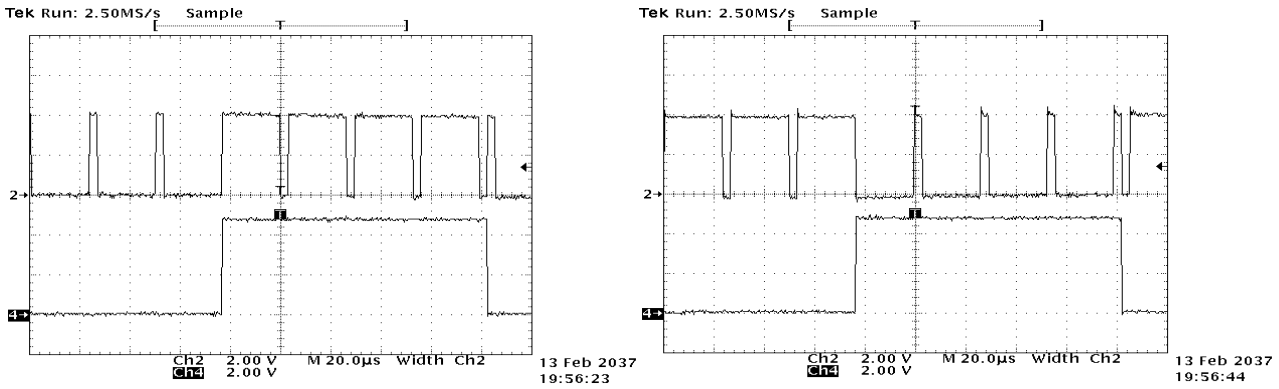


Figure 14. Positive and negative polarity serration-type CSYNC

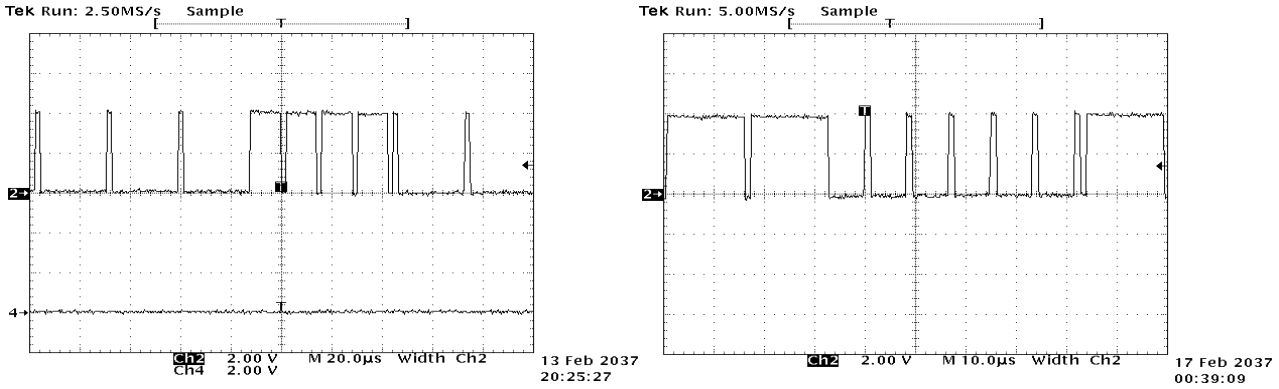


Figure 15. Positive and negative polarity "serration with equalization"-type CSYNC

Sync-On-Green (Analog Composite Sync)

The gm5020 supports standard implementations of both OR/AND type and XOR type SOG signals. The voltage level of the sync tip during the vertical sync period can range from -0.3V to –0.15V.

4.3.4 Clock Recovery

The SDDS (Source Direct Digital Synthesis) clock recovery circuit generates the clock used to sample analog RGB data (IPCLK or source clock). This circuit is locked to HSYNC (or recovered HSYNC in the case of CSYNC/SOG inputs) of the incoming video signal.

Patented digital clock synthesis technology makes the gm5020 clock circuits resistant to temperature/voltage drift. Using DDS (Direct Digital Synthesis) technology, the clock recovery circuit can generate any IPCLK clock frequency within the range of 10MHz to 162MHz.

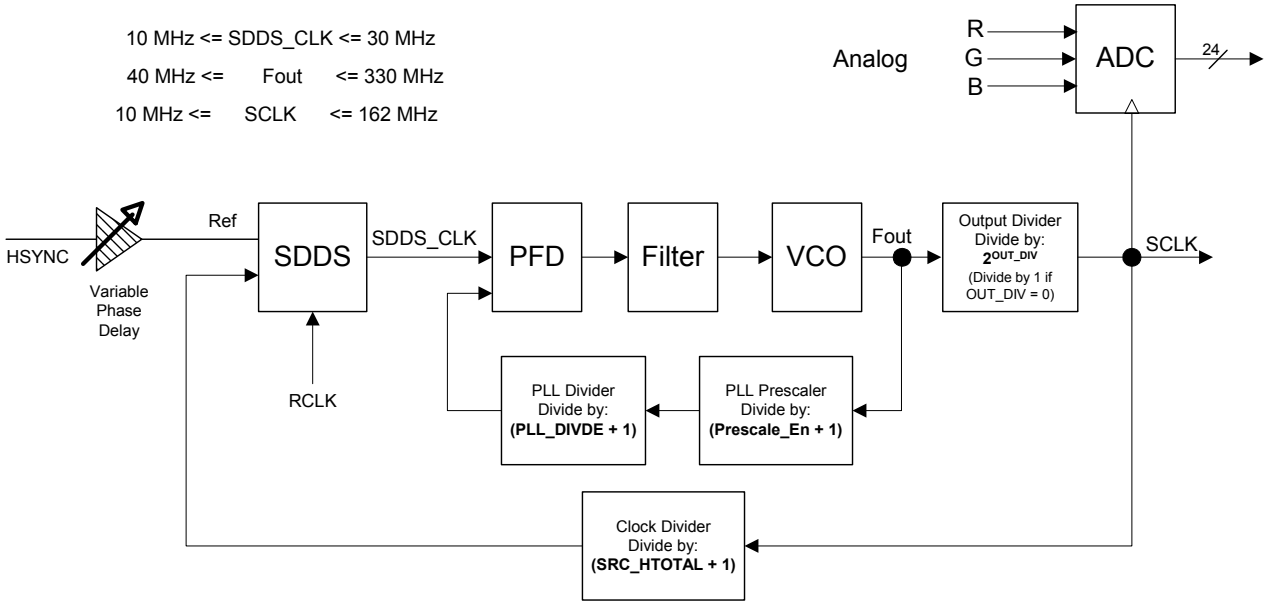


Figure 16. gm5020 Clock Recovery

4.3.5 Sampling Phase Adjustment

The ADC sampling phase is adjusted by delaying the HSYNC input to the DDS through a variable phase delay. This block was designed in a way to be temperature/voltage insensitive and to exhibit nominally zero phase drift. The following curve represents the nominal total delay through the block as a function of programming.

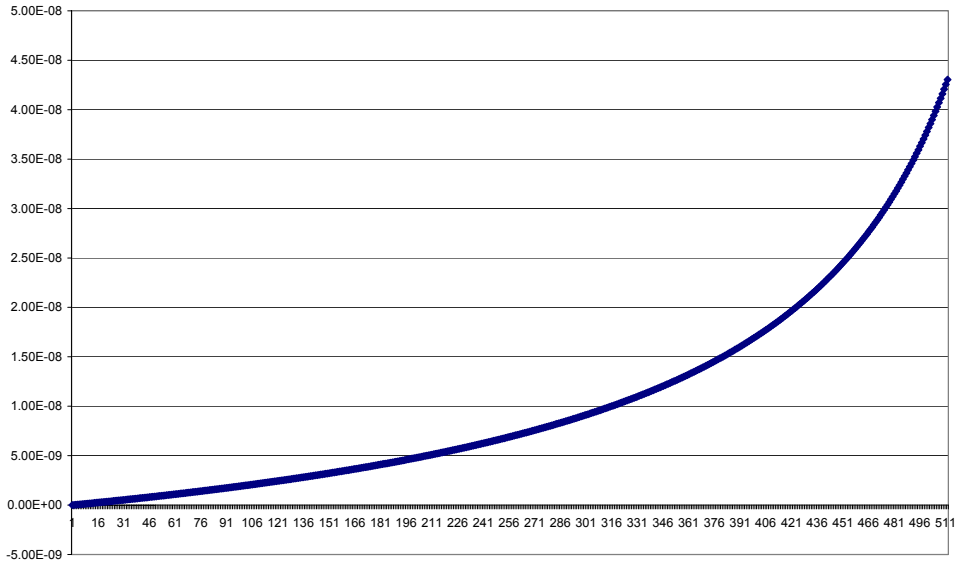


Figure 17. Phase Adjustment Delay Curve

It is common for LCD monitor applications for the end user to change the sampling phase in equally stepped intervals. Equally spaced time delays can be implemented using several programming techniques:

1) LUT approach. A look-up-table is developed with entries representing equally spaced time delays. Multiple LUTs or changing the step size within a LUT can be used to increase the quantization of the time delay. The Genesis firmware utilizes a LUT with 150ps entries and changes the step size depending on the mode detected. This is the recommended method.

2) Piece-wise linear connected lines. In this case, the resultant curve can be approximated with a number of line segments connected vertix-to-vertix. The firmware would be responsible to select the appropriate line (and therefore the appropriate equation) based on total delay required. Please contact Genesis for line equations if required.

4.4 Ultra-Reliable Digital Visual Receiver (DVI Rx)

The Ultra-Reliable DVI receiver block of the gm5020 is compliant with DVI1.0 single link specifications. Digital Visual Interface (DVI) is a standard that uses Transition Minimized Differential Signaling protocol (TMDS). This block supports an input clock frequency ranging from 20 MHz to 165 MHz.

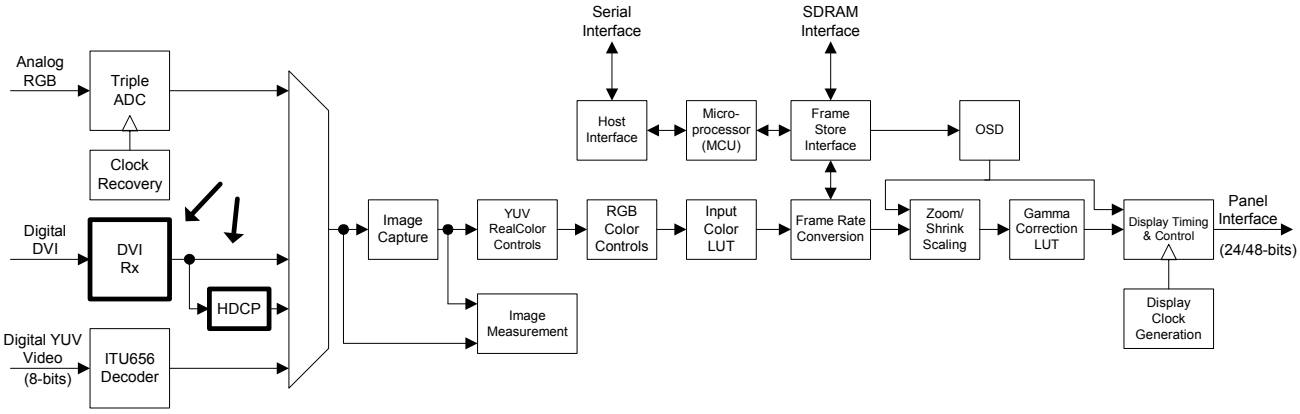


Figure 18. DVI Block

4.4.1 DVI Receiver Characteristics

Table 12 summarizes the characteristics of the four Receiver Pair inputs. Please note that it is very important to follow the recommended layout guidelines for these signals. These are described in "gm5020/5060 System Layout Guidelines" document number C5020-APN-01D.

Table 12. DVI Receiver Characteristics

	MIN	TYP	MAX	NOTE
DC Characteristics				
Differential Input Voltage	150mV		1200mV	
Input Common Mode Voltage	AVDD –300m V		AVDD -37mV	
Behavior when Transmitter Disable	AVDD -10mV		AVDD +10mV	
AC Characteristics				
Input clock frequency	20 MHz		165 MHz	
Input differential sensitivity (Peak-to-peak)	150mV			
Max differential input (peak-to-peak)			1560 mV	
Allowable Intra-Pair skew at Receiver			250 ps	Input clock = 165 MHz
Allowable Inter-Pair skew at Receiver			4.0 ns	
Worst case differential input clock jitter tolerance			188 ps	

Through register programming, the receiver unit may be placed in one of three states:

- **Active:** The receiver block is fully on and running.
- **Standby:** Only the RXC channel remains active. Data and other control signals are not decoded.
- **Off:** The receiver block is powered down.

4.4.2 HDCP (High-Bandwidth Digital Content Protection System)

Note: This section refers only to the gm5020-H chip.

The HDCP system allows for authentication of a video receiver, decryption of encoded video data at the receiver, and renew-ability of that authentication during transmission. The gm5020-H implements circuitry to allow for authentication and decryption of video as specified by the HDCP 1.0 protocol for DVI inputs.

For enhanced security, Genesis provides a means of storing and accessing the secret key given to individual monitor units in an encrypted format.

Further details of the protocol and theory of the system can be found in the *High-bandwidth Digital Content Protection System* specification, proposed by Intel Corporation.

4.5 ITU-R BT656 Video Input

The gm5020 accepts an 8-bit YCbCr 4:2:2 video data stream conforming to ITU-R BT656 (D-1) standards. For further details on the ITU-R BT656 specification, see www.itu.int.

The data and the 27 MHz sampling clock are provided by an external video decoder. The ITU-R BT656 format provides no separate horizontal or vertical sync (HSYNC, VSYNC) to the gm5020. The active window is not programmed. Rather, it is interpreted from codes embedded in the data stream.

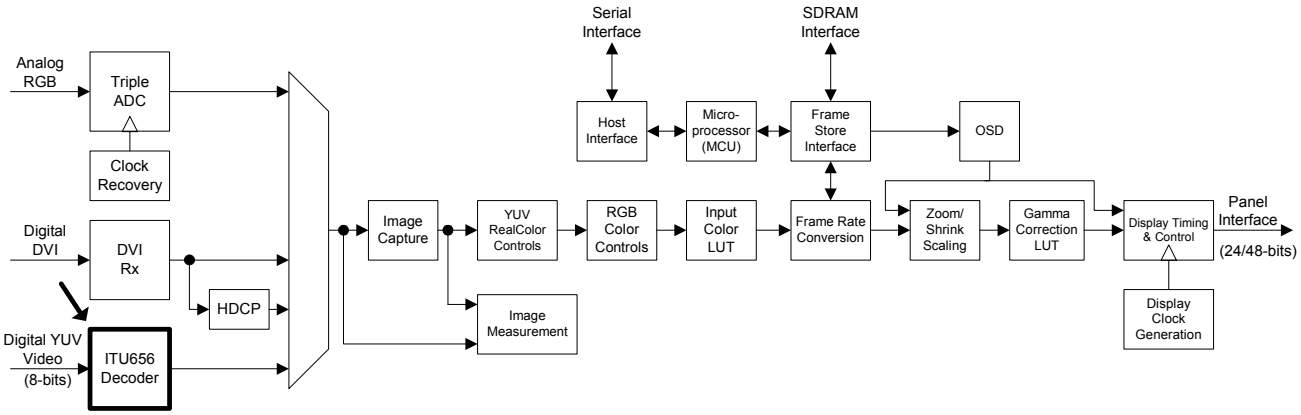


Figure 19. ITU-R BT656 Block

4.5.1 YCbCr Input Clamping

YCbCr input to the gm5020 is always automatically clamped to restrict the input data to ITU-R BT601 levels:

Y Bottom clamping:	Y data < 16 is clamped to 16.
Y Top clamping:	Y data > 235 is clamped to 235.
CbCr Bottom clamping:	CbCr data < 16 is clamped to 16.
CbCr Top clamping:	CbCr data > 240 is clamped to 240.

4.6 Image Capture – Active Window Decoder

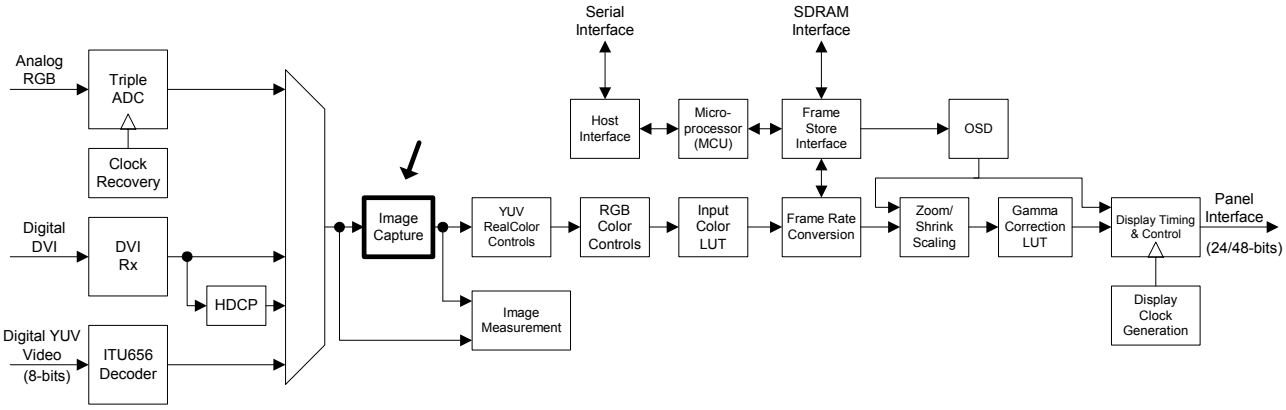


Figure 20. Image Capture Block

The gm5020 Active Window Decoder (AWD) is responsible for identifying "active" or "non-blanking" data to the subsequent blocks in the gm5020. Only active data is processed by the chip. There are several programming methods of the AWD based on the selected input. These are described below.

The maximum number of active pixels per line is 2047, the minimum is 50 pixels. The maximum number of active lines per input field is 2047, the minimum is 50 lines. The maximum number of total pixels per line including blanking is 4096. The maximum number of total lines per input field including blanking is 2048.

4.6.1 ADC Capture Window

Figure 21 below illustrates the capture window used for the ADC input. In the horizontal direction the capture window is defined in IPCLKs (equivalent to pixel counts). In the vertical direction it is defined in lines.

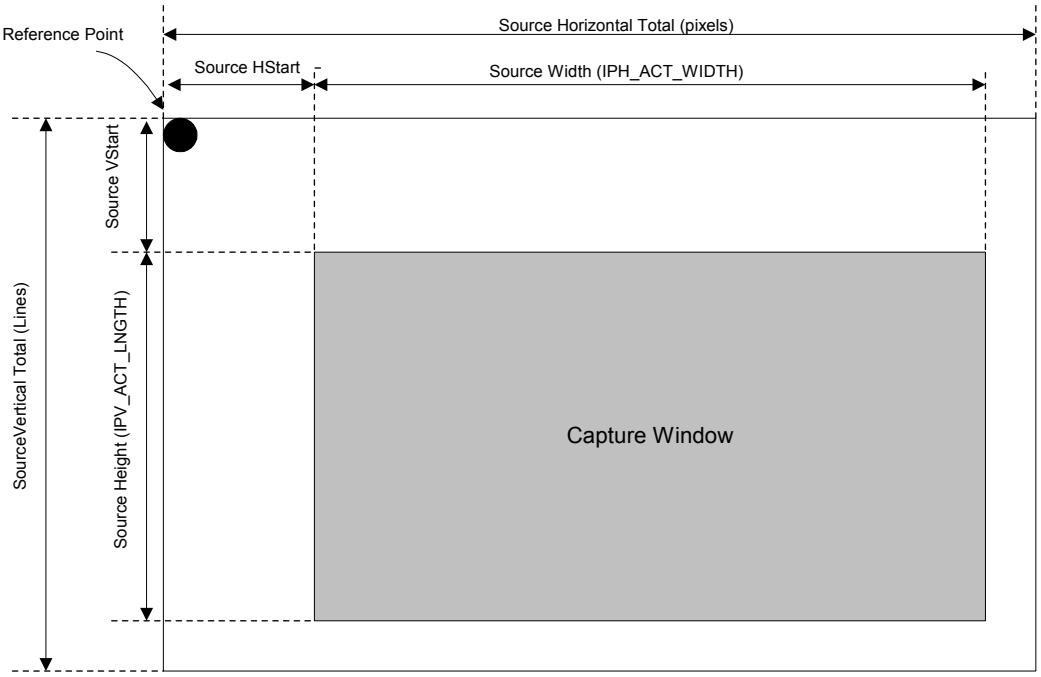


Figure 21. Capture Window

The Reference Point marks the leading edge of the first internal HSYNC following the leading edge of an internal VSYNC.

Horizontal parameters are defined in terms of single pixel increments relative to the internal horizontal sync. Vertical parameters are defined in terms of single line increments relative to the internal vertical sync.

4.6.1.1. HSYNC / VSYNC Delay

The active input region captured by the gm5020 is specified with respect to internal HSYNC and VSYNC. By default, internal syncs are equivalent to the HSYNC and VSYNC driven in at the selected input port, and forces the captured region to be bounded by HSYNC and VSYNC timing. The gm5020 provides an internal HSYNC and VSYNC delay capability for ADC inputs, which removes this limitation. By delaying the sync seen internally, the gm5020 can capture data which actually spans across the sync.

Modifying the HSYNC and VSYNC delay parameters will modify the data selected by the AWD. This is the preferred method to implement image positioning.

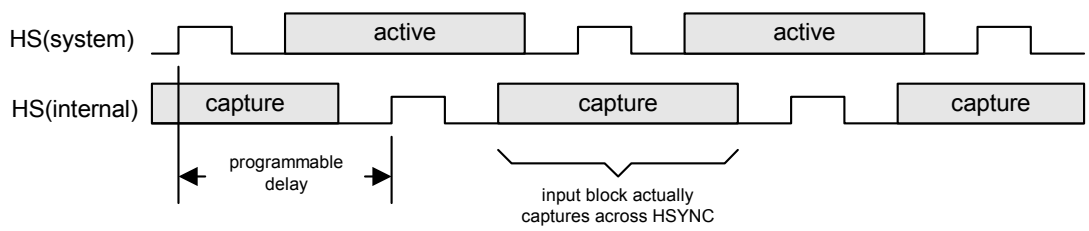


Figure 22. HSYNC Delay

Delayed horizontal sync may be used to solve a potential problem with VSYNC jitter with respect to HSYNC. VSYNC and HSYNC are generally driven coincidentally, but may arrive at slightly different times to the gm5020 because of different conditioning at the PCB level. As a result, VSYNC may be seen earlier or later, or possibly jitter relative to HSYNC. Because VSYNC is used to reset the line counter and HSYNC is used to increment it, any difference in the relative position of HSYNC and VSYNC is seen on-screen as vertical jitter. By delaying the HSYNC a small amount, it can be ensured that VSYNC will always reset the line counter prior to it being incremented by the "first" HSYNC.

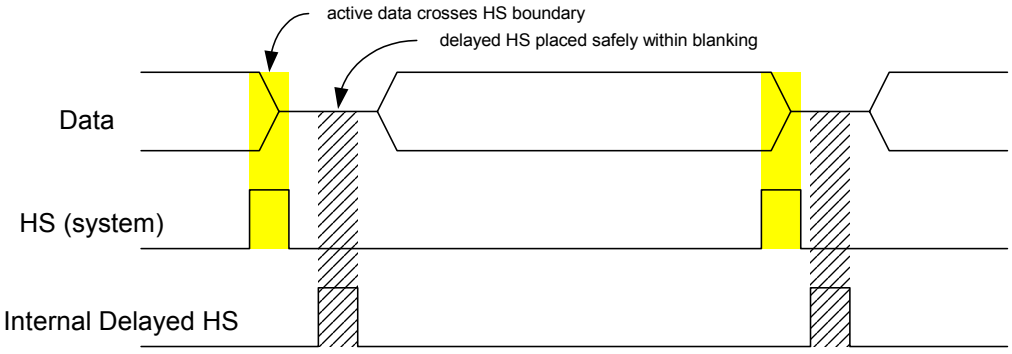


Figure 23. Active Data Crosses HSYNC Boundary

4.6.2 DVI Capture Window

DE (Display Enable), HSYNC and VSYNC are synthesized internally (regenerated) by examining the active regions of each line and compensating for possible source timing errors and/or embedded HSYNC / VSYNC jitter.

There are two modes of operation available to define the active window for DVI inputs: DE mode and CREF mode.

DE Capture Mode - In this mode the AWD considers the display enable (DE) code embedded in the DVI signal, and uses it explicitly to define the active window. The programmed horizontal and vertical active start parameters are ignored by the AWD. The horizontal active width and vertical active length parameters must still be programmed.

CREF Capture Mode - In this mode the regenerated DE signal is ignored and the active window is programmed in the same manner as the ADC inputs (See Section 4.6.1.)

4.6.3 ITU-R BT656 Capture Window

The input port extracts the active data, field type, and the horizontal and/or vertical blanking embedded in the input stream. Note that Cb and Cr (shown in the figure below) correspond to U and V respectively. The extracted data is converted to 24-bit YCbCr 4:4:4 format.

Horizontal and vertical sync signals required for Input Lock Event timing are internally generated in this case.

Though the AWD is effectively operating in DE-capture mode (See Section 4.6.2 above), it is still possible to "crop" the image. This is described in the application note C5020-APN-12.

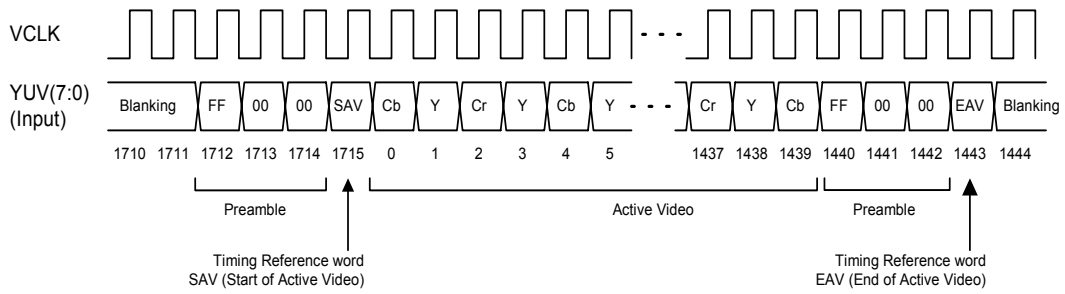


Figure 24. ITU-R BT656 Input

4.7 Image Measurement

The gm5020 has various measurement resources. The types of measurement can generally be grouped into format measurement and data measurement.

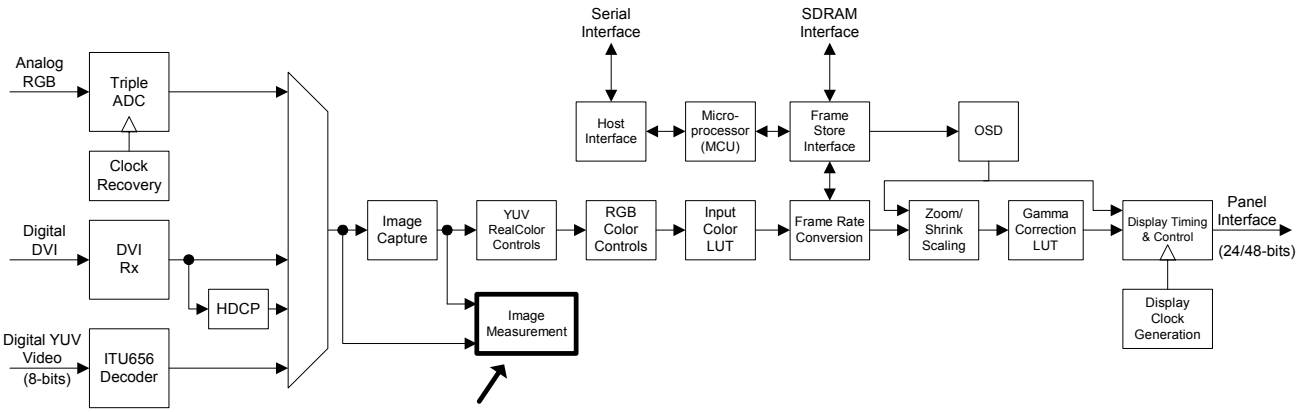


Figure 25. Image Measurement Block

4.7.1 Input Format Measurement (IFM)

The gm5020 has an Input Format Measurement block (the IFM) providing the capability of measuring the horizontal and vertical timing parameters of the input video source. This information may be used to determine the video format and to detect a change in the input format. It is also capable of detecting the field type of interlaced formats.

The IFM features a host programmable reset, separate from the regular gm5020 soft reset. The IFM is capable of operating while the rest of the gm5020 is running in power down mode.

Horizontal measurements are measured in terms of the selected IFM_CLK (either T_CLK or R_CLK/4). The IFM is able to measure the horizontal period and active high pulse width of the HSYNC signal, in terms of the selected clock period (either T_CLK or R_CLK/4.). Horizontal measurements are performed on only a single line per frame (or field). The line used is programmable.

The IFM is able to measure the vertical period and VSYNC pulse width in terms of rising edges of HSYNC. When using C-SYNC or sync-on-green input mode, these measurements use internally synthesized HSYNC and VSYNC signals.

Once enabled, measurement begins on the rising VSYNC and is completed on the following rising VSYNC. Measurements are made on every field / frame until disabled.

The skew between HSYNC and VSYNC is also able to be determined. The skew is important to determine in situations where the HSYNC and VSYNC signals are nearly edge-coincident. Vertical measurements begin and end with consecutive VSYNC signals, however, nearly coincident HSYNC edges provides the opportunity for +/-1 jitter results in the VSYNC

measurements. In the case the edges are nearly coincident, the HSYNC signal may be optionally delayed by 16 clock cycles to avoid any jitter in the results.

4.7.1.1. Format Change Detection

The IFM is able to detect changes in the input format relative to the last measurement and then alert both the system and the embedded microprocessor. The microprocessor sets a measurement difference threshold separately for horizontal and vertical timing. If the current field / frame timing is different from the previously captured measurement by an amount exceeding this threshold, a status bit is set. An interrupt can also be programmed to occur.

4.7.1.2. Watchdog

The watchdog monitors input VSYNC / HSYNC. When any HSYNC period exceeds the programmed timing threshold (in terms of the selected IFM_CLK), a register bit is set. When any VSYNC period exceeds the programmed timing threshold (in terms HSYNC pulses), a second register bit is set. An interrupt can also be programmed to occur. These watchdog status bits are used to identify if the input source has been removed.

4.7.1.3. Internal Odd/Even Field Detection (For Interlaced Inputs to ADC Only)

The IFM has the ability to perform field decoding of interlaced inputs to the ADC. The user specifies start and end values to outline a "window" relative to HSYNC. If the VSYNC leading edge occurs within this window, the IFM signals the start of an ODD field. If the VSYNC leading edge occurs outside this window, an EVEN field is indicated (the interpretation of odd and even can be reversed). The window start and end points are selected from a predefined set of values.

For ADC interlaced inputs, the gm5020 may be programmed to automatically determine the field type (even or odd) from the VSYNC/HSYNC relative timing.

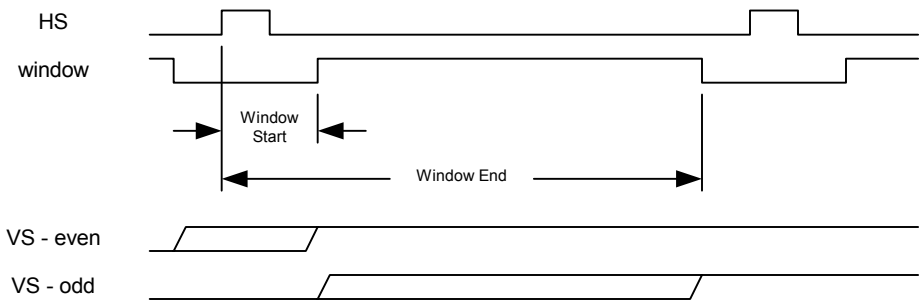


Figure 26. ODD/EVEN Field Detection

Note: ITU-R BT656 inputs do not require the above field detection feature; the field type is embedded in the data stream.

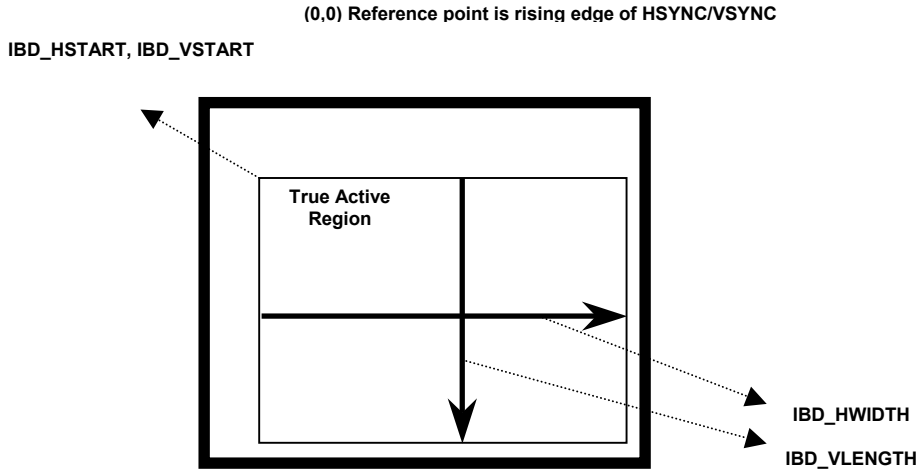
4.7.2 Input Data Measurement

The gm5020 provides a number of pixel measurement functions intended to assist in configuring system parameters such as pixel clock, sample clocks per line, sampling phase, centering the image, or adjusting the contrast and brightness.

4.7.2.1. Input Boundary Detection

Since there is no DE signal present in the analog source, the data from the ADC must be examined to determine when the active data starts and ends. The Input Boundary Detection block (IBD) measures and identifies the vertical and horizontal active region within the input data stream.

IBD monitors the input data throughout the frame to locate the first and last pixels exceeding a programmable threshold. The vertical and horizontal locations are latched into corresponding registers at the conclusion of each frame during the VSYNC interval. Horizontal results are in terms of pixels while vertical results are in terms of lines. Correct results require the input image to have at least one pixel of boundary on each edge.



4.7.2.2. Sum of Differences Measurement

The gm5020 contains a feature called Sum of Differences. The Sum of difference feature compares consecutive pixel values to a programmable threshold, adding the absolute-valued difference to an accumulator when the difference exceeds the threshold. The process occurs over the entire active region - the total number of summations equal to (number of horizontal active pixels – 1) x (number of vertical active pixels). The results are latched during the VSYNC interval and the accumulator is reset. The sum of difference feature is normally used to determine the correct ADC sampling phase.

$$SUMDIFF = \sum \left| P_N - P_{N-1} \right|$$

4.7.2.3. Image Minimum/Maximum

The gm5020 performs measurements on the input data that is used to adjust brightness and contrast. The MINMAX registers return the minimum or maximum Red/Green/Blue pixel values in the programmed active region. In practice, if the active region is reduced in size, they provide a less sensitive alternative to the ADC overflow and underflow flags.

4.7.2.4. Pixel Grab

A single pixel anywhere in a frame may be captured for analysis. The pixel is specified in qualified clocks relative to the selected input port HSYNC and VSYNC leading edges. Red, green and blue intensity values are returned in separate registers. This function is used to provide precise pixel information when determining the correct sampling phase at very high frequencies.

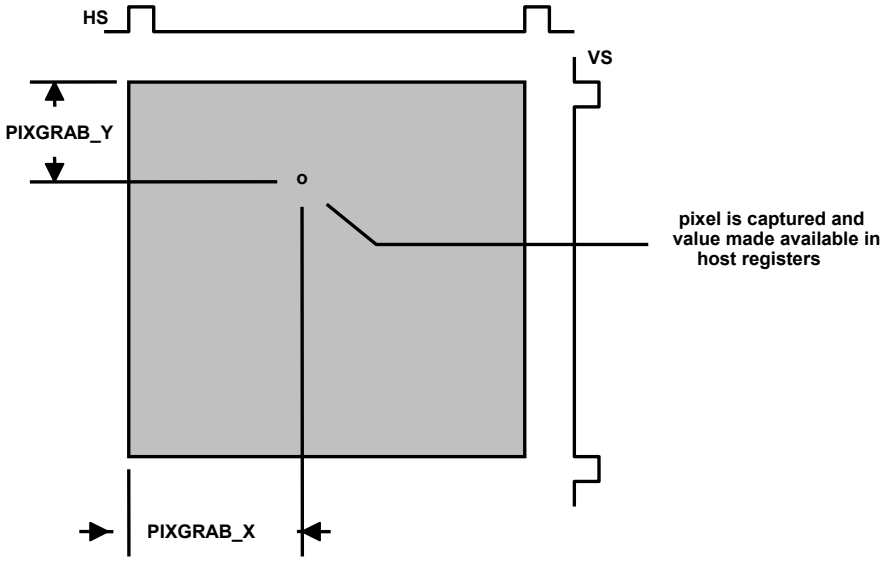


Figure 27. Pixel Grab

4.8 Digital Color Controls

The gm5020 provides digital adjustment of the captured image data, allowing control over the image black level, contrast, brightness, hue and saturation.

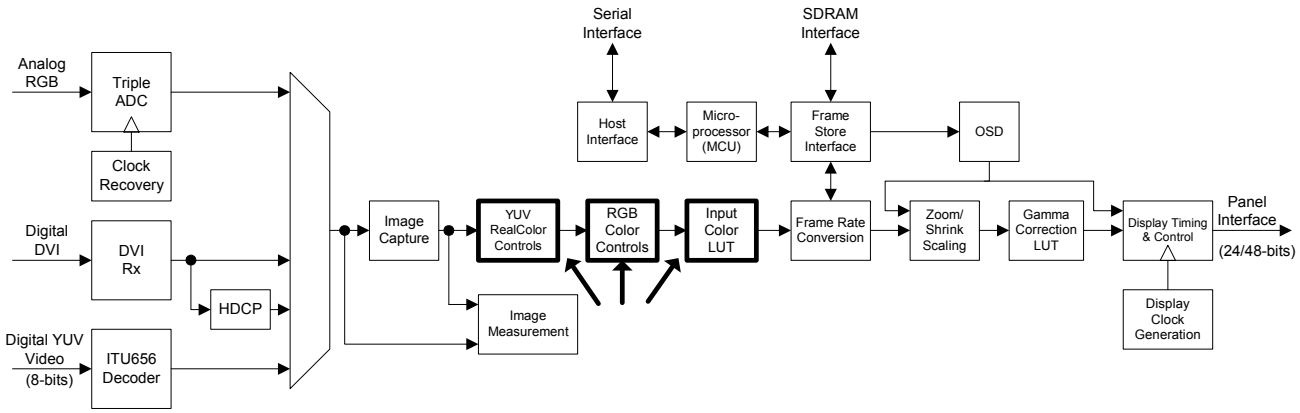


Figure 28. Digital Color Control Blocks

4.8.1 YUV Hue / Saturation Controls

Color adjustment can be performed in the CbCr domain. These controls are available for RGB graphics input as well as for the CbCr video input. By default these functions are disabled, and color adjustment is not performed.

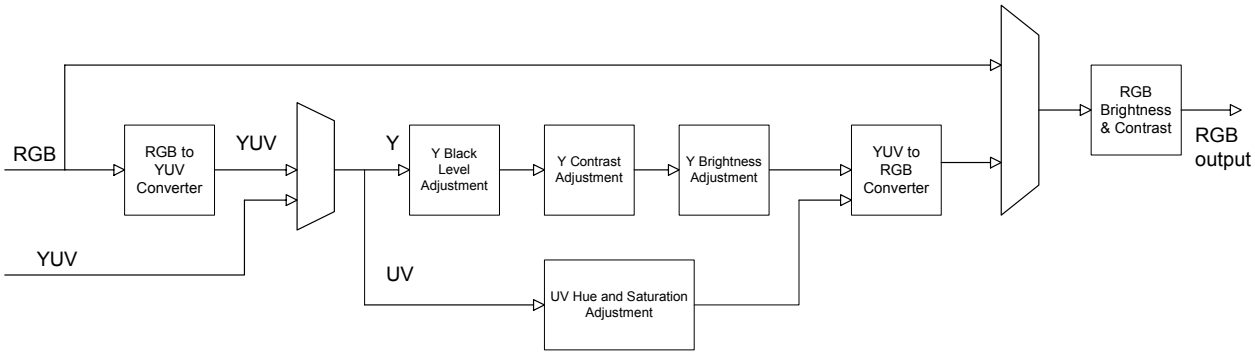


Figure 29. YUV Color Controls

The functions are defined as follows:

Hue is a pure rotation of the CbCr (color) vector through an angle.

Saturation is a multiplicative factor applied to both Cb and Cr equally.

Contrast is a multiplicative factor applied to Y.

Brightness is an additive factor applied to Y.

The equations for these controls are as follows:

Y(out) = (Y - YBlackLevel) * Contrast + Brightness

Cb(out) = (Cb * cos(Hue) + Cr * sin(Hue)) * Saturation = Cb * Sat*cos(Hue) + Cr * Sat*sin(Hue)

Cr(out) = (Cr * cos(Hue) - Cb * sin(Hue)) * Saturation = Cr * Sat*cos(Hue) - Cb * Sat*sin(Hue)

Parameters are used directly in the associated multiplication and summation operations as programmed.

4.8.2 RealColor Flesh tone Adjustment

The human eye is more sensitive to variations of flesh tones than other colors; for example, the user may not care if the color of grass is modified slightly during image capture and/or display. However, if skin tones are modified by even a small amount, it is unacceptable. The gm5020 features flesh tone adjustment capabilities. This feature is not based on lookup tables, but rather a manipulation of YUV-channel parameters. Flesh tone adjustment is available for all inputs.

4.8.3 RGB Black Level / Contrast / Brightness

The black level adjustment is a subtractive stage, lowering each input pixel by a programmable value. This may be used to adjust the baseline black value of the input data.

R(out) = (R - RedBlackLevel) * RedContrast + RedBrightness
G(out) = (G - GreenBlackLevel) * GreenContrast + GreenBrightness
B(out) = (B - BlueBlackLevel) * BlueContrast + BlueBrightness

For example, if the lowest valued pixel expected to be encountered is 16, then 16 could be subtracted from all input pixels, making the pixel value 16 (or lower) black. The desired black level is maintained through the following contrast (multiplicative) stage.

The contrast adjustment increases or decreases the slope of the input / output function as shown below.

The brightness adjustment is a straight additive stage, increasing each pixel value by a programmed amount (saturating at 255).

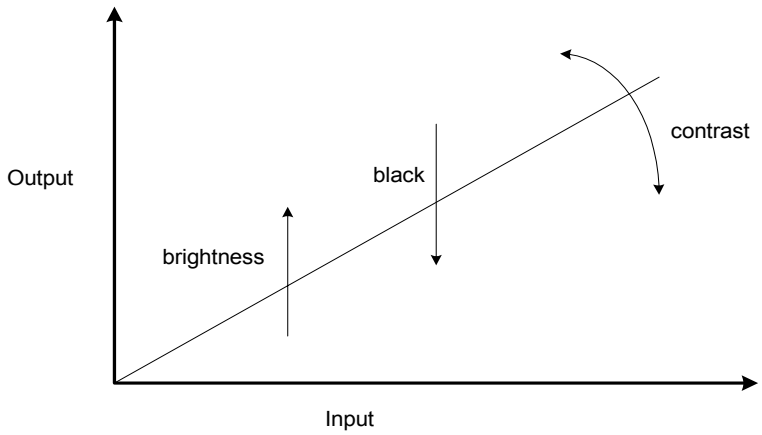


Figure 30. Black / Contrast / Brightness Transfer Function

4.8.4 Input Look-up Table

After RGB color adjustment, a LUT may be optionally enabled. The LUT produces 10-bit output data for each of 256 input locations. There is a separate table for each red, green and blue channel. Data is written to the input LUT through the host interface. The three channels may be written independently or simultaneously with the same values.

Although the LUT produces 10-bit output, the FRC/Scaler blocks that follow utilize an 8-bit data path. Therefore, a dithering function is performed to increase the bit-depth. Both random-type and ordered-type dithering methods are available.

The primary use for the input LUT is to perform moire cancellation. This is further described in Section 4.12.2. Please contact Genesis for appropriate software to determining the LUT entries when implementing this function.

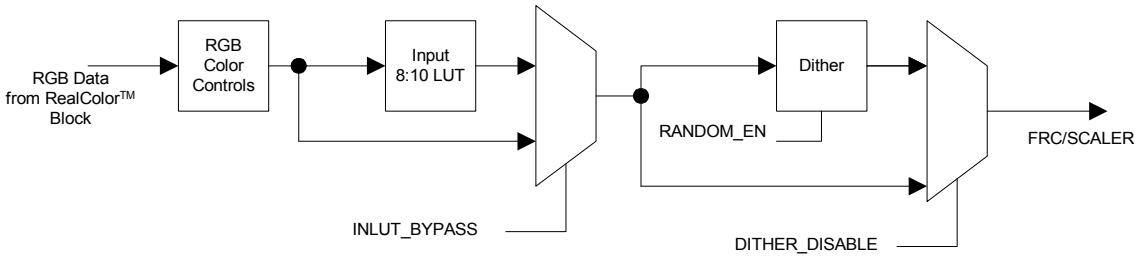


Figure 31. Input LUT and Dithering

4.9 Horizontal Shrink

A shrink function may be optionally performed on the input data prior to being stored in the DRAM. The shrink feature allows an arbitrary horizontal active resolution reduction to between (50% + 1 pixel) to 100% of the input. For example, SXGA 1280 pixels may be scaled and displayed as XGA 1024 pixels. Shrinking the image prior to frame-rate conversion reduces the bandwidth required in the DRAM interface. Note that horizontal shrink and horizontal zoom (See Section 4.12) cannot be performed simultaneously. Note also that the pre-filter OSD overlay occurs after horizontal shrink has been performed.

4.10 Frame Store Interface

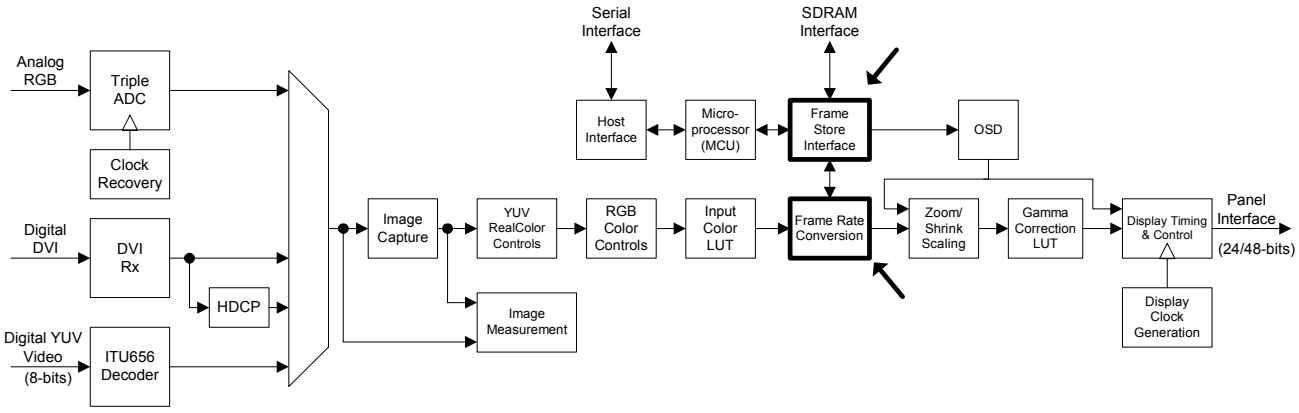


Figure 32. Frame Store Interface Blocks

The external frame buffer provides the storage required for the frame rate conversion process and the integrated OSD. The gm5020 is able to operate with 16Mbit or 64Mbit Synchronous DRAM (SDRAM) devices and/or 16Mbit or 32Mbit Synchronous Graphics RAM (SGRAM) devices. The FRC data bus width is programmable to 32 or 48-bits. Generally, 32 bits is sufficient for XGA and 48 bits is sufficient for SXGA.

The Frame Rate Conversion Block may be bypassed for applications not requiring frame rate conversion. See Section 4.14.

4.10.1 Supported SDRAM Devices

The gm5020 operates seamlessly with commercially available SDRAM / SGRAM devices at operating frequencies up to 143MHz. Practically, a 120 MHz clock frequency is sufficient for typical LCD Monitor applications. For XGA operation the frame store is 32 bits wide (e.g. two 1Mx16 devices). For SXGA operation the frame store is 48 bits wide (e.g. three 1Mx16 devices).

4.10.2 Adjustable Frame Store Interface Delays

The interface setup/hold times and propagation delay to the external DRAM can be adjusted. This is done by programming registers to achieve the timing values indicated in Section 5.2 (IO timing for FSC).

4.10.3 Frame Store Bandwidth Requirements

All data coming into and flowing out of the gm5020 frame rate converter must pass through the frame store interface. Therefore, this interface must provide enough bandwidth to support the combined bandwidth demands of the input and display ports.

The table below summarizes the required memory for single buffering and frame store bandwidth for various input formats, not including extra memory required for OSD. It also details the number of memory devices needed and the prevalent DRAM configurations. In all cases the output is assumed to be SXGA 60Hz.

Table 13. Framestore Bandwidth and Data Widths for Various Formats

Input Format	Input Pixel Clock (MHz)	Required DRAM Storage (Mbits) [3]	Required DRAM Bandwidth (Mbits/s) [1][2]	DRAM Configuration		
				Speed (MHz)	Data Width (bits)	Devices
SXGA 85Hz	158	31.5	6282[4]	120[4]	48	1 @ 1M x 16 and 1 @ 1M x 32 **OR** 3 @ 1M x 16
SXGA 75 Hz	135	31.5	5802	120	48	1 @ 1M x 16 and 1 @ 1M x 32 **OR** 3 @ 1M x 16
SXGA 60 Hz	108	31.5	5082	120	48	1 @ 1M x 16 and 1 @ 1M x 32 **OR** 3 @ 1M x 16
XGA 85 Hz	95	18.9	3841.2	120	32	2 @ 1M x 16 **OR** 1@ 1M x 32
XGA 75 Hz	79	18.9	3321.4	120	32	2 @ 1M x 16 **OR** 1@ 1M x 32
XGA 60 Hz	65	18.9	3054.5	120	32	2 @ 1M x 16 **OR** 1@ 1M x 32

NOTE 1: Horizontal shrink is not considered in this table. When enabled, horizontal shrink reduces the required bandwidth.

NOTE 2: The display frame rate is assumed to be 60 Hz.

NOTE 3: The input is assumed to be “single-buffered” in the DRAM

NOTE 4: The input is captured at SXGA 85Hz but is line spread to allow lower internal operating frequency. This allows for the 120MHz frame rate clock.

The FCLK PLL synthesizes the F_CLK to drive the FRC logic and Framestore Interface Clock. The FCLK PLL must be programmed such that: F_CLK < (DCLK x 3). This restriction should impose no functional limitations.

4.10.4 SDRAM Power On Sequence

SDRAM devices have a power-on sequence that must be performed before they can be reliably accessed. This consists of a pre-charge cycle, 20 refresh cycles, and a MRS cycle. (The MRS – mode register setting – programs the DRAM for burst size, access latency, etc.) The gm5020 automatically performs this sequence.

4.10.5 SDRAM Power Down

SDRAM devices typically have a low power, non-operational mode. The gm5020 supports this feature by providing a power down sequence controller, enabled via a host-programmed register. This feature should always be used before disabling the framestore interface. A soft reset is required after bringing the SDRAMs back from power-down mode.

4.10.6 Pan and Crop Operations

Pan and Crop is a function that may be implemented in the Active Window Decoder or via the frame store controller. The frame store controller may be programmed to extract a rectangular portion of the stored image. This rectangular portion of the image may be displayed at native resolution, or scaled to the display resolution. Note that frame tear may result if a single frame buffer is used.

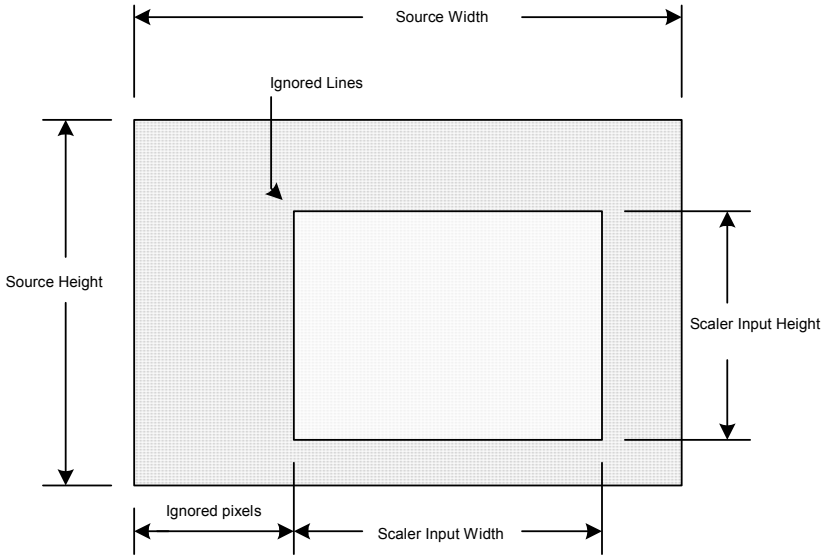


Figure 33. FRC Required Parameters

It is normally the practice to utilize the AWD for cropping when using ADC inputs and DVI inputs with CREF capture.

4.10.7 Double Buffering Frame Store Bandwidth Requirements

To perform pan, crop and/or flip operations without frame tear, the frame store must be large enough to accommodate two images (double buffering). For example, if the input is SXGA resolution, the frame store must be a minimum of 1280 x 1024 x 24-bits x 2 = 60 Mbits.

4.10.8 Freeze Frame

Freeze frame capability is made available by disabling the input capture during the vertical blanking interval. This does not disrupt the flow of data from the frame store. During freeze frame, adjusting the contrast and brightness controls will have no affect on the displayed image.

4.10.9 Interlaced Formats and De-interlacing

The FRC is able to accept vertically interlaced images. These images may be de-interlaced using a static mesh technique. Static mesh de-interlacing takes lines from an odd and even field pair and meshes them together, doubling the number of output lines. This technique is often used to de-interlace static graphics inputs.

4.11 Scaling

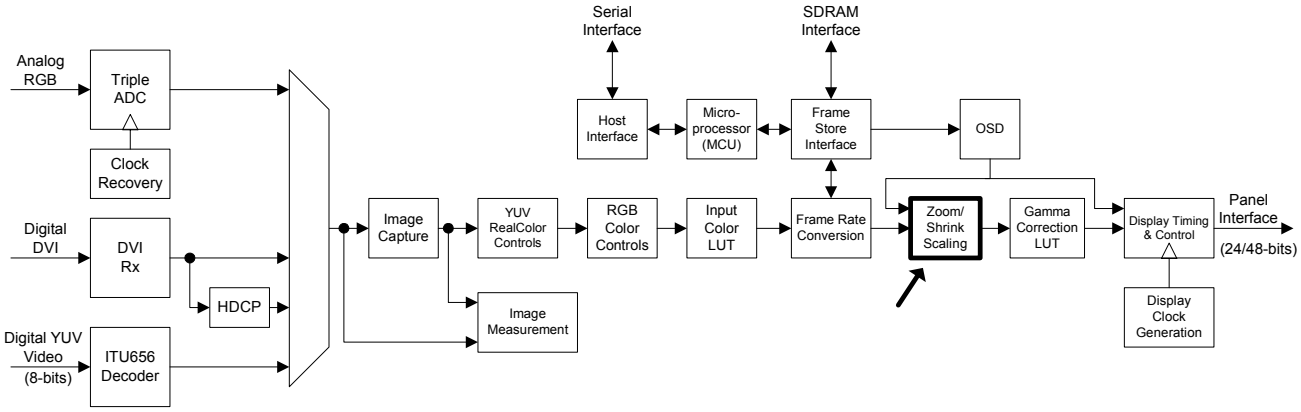


Figure 34. Scaling Block

The gm5020 zoom (expansion/magnification) scaler uses an advanced third generation multi-tap FIR filter technique proprietary to Genesis Microchip Inc., and provides high quality scaling of real time video and graphics images. An input field/frame is scalable in both the vertical and horizontal dimensions.

Interlaced fields may be spatially de-interlaced by vertically scaling and repositioning the input fields to align with the output display's pixel map.

4.11.1 Pixel Replication Scaling

In addition to advanced FIR filtering, the gm5020 scaling filter can combine a 2x pixel-replication type scaling function. This is useful for improving the sharpness and definition of graphics when scaling at high zoom factors (such as VGA to SXGA). Replication is available in both the horizontal and vertical directions and may be combined with the FIR filter for greater than 2x scaling.

4.11.2 Vertical Shrink

The gm5020 also provides an arbitrary vertical shrink down to (50% + 1 line) of the original image size. Together with the arbitrary horizontal shrink, this allows the gm5020 to capture and display images one VESA standard format larger than the native display resolution. For example, SXGA may be captured and displayed on an XGA panel.

4.11.3 Adaptive Contrast Enhancement (ACE)

When zoom scaling is enabled, the gm5020 features the ability to sharpen text and graphic images. This is performed on an adaptive basis by detecting pulse and step functions on the input, and effectively adjusting filter coefficients.

The ACE filter provides benefit in some limited scaling ratios:

- Scaling from SVGA input resolution to XGA output resolution
- Scaling from XGA input resolution to SXGA output resolution

4.12 Gamma Correction LUT

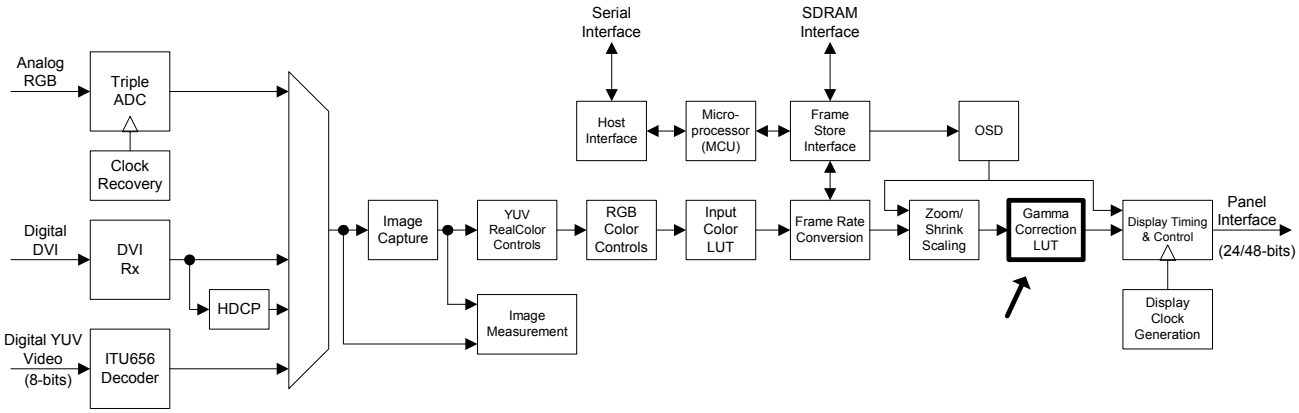


Figure 35. Gamma Correction LUT Block

After the scaling block, the gm5020 provides an 8 to 10-bit look up table (LUT) for each input color channel. Although any arbitrary transfer function may be programmed, this LUT is primarily used for two purposes: Gamma correction of the display device and moire cancellation.

A 10-bit output results in an improved color depth control. The 10-bit output is optionally dithered down to 8 bits (or 6 bits) per channel at the display. Dithering works by spreading quantization error over neighboring pixels both spatially and temporally. The benefit of dithering is that the human eye will tend to average neighboring pixels and a smooth image free of contours will be perceived. Both ordered-type and random-type dithering methods are available, though ordered-type is preferred to optimize quality.

The LUT has a host programmable bypass enable. If bypassed, the LUT does not require programming.

As was the case with the input LUT, Data is written through the host interface. The three channels may be written independently or simultaneously with the same values.

4.12.1 Gamma Correction

Screen brightness is a function of the voltage applied to the LCD display. A “gamma” effect will occur when the change in brightness is different from an increase in applied voltage at low magnitude versus the same voltage increase at high magnitudes. LCD displays typically characterize this non-uniform behavior with a “Gamma Curve”. A typical curve is shown below.

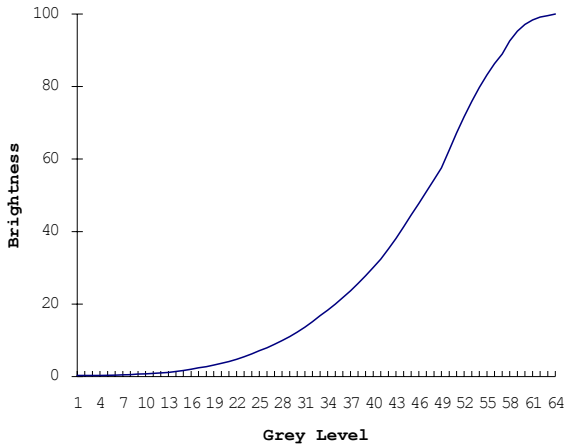


Figure 36. Gamma Response Curve

The gm5020 Gamma Correction LUT may typically be programmed with an inverse function to compensate for the gamma effect.

4.12.2 Moiré Cancellation

The “moire” effect occurs as a result of resampling (scaling) the input image to a different display resolution. The effect occurs independantly of the scaler implementation. The effect typically is most noticeable in regions of high switching and generally more objectionable when realizing complex scaling ratios (eg. 800 pixels scaled to 1024 represents a scaling ratio of 32/25 and a more noticeable effect than 1024 pixels scaled to 1280 with a scaling ratio of 5/4).

By utilizing both the input and gamma LUTs, the moire effect can be reduced or eliminated. This proprietary method is handled by G-Wizard software available from Genesis Microchip.

4.13 Display Timing and Control

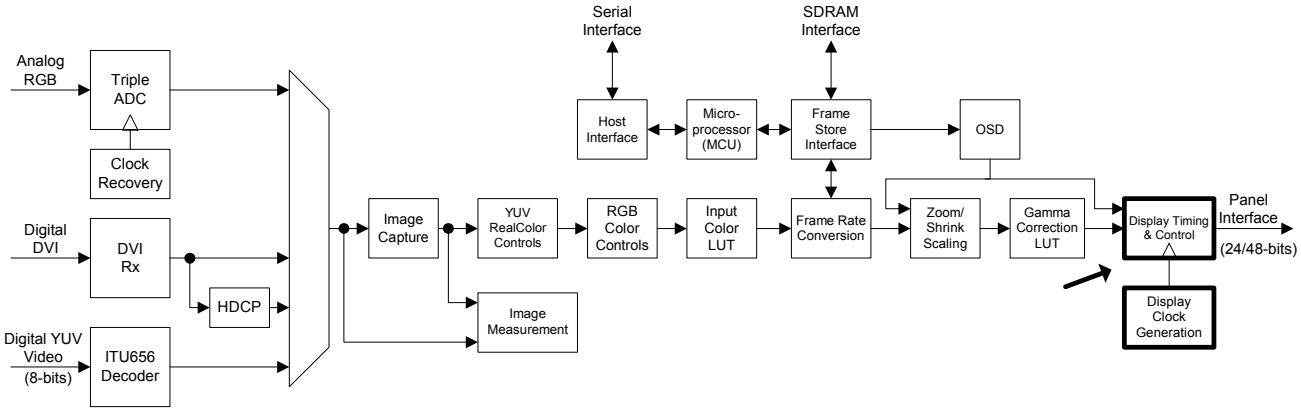


Figure 37. Display Timing and Control Blocks

The Display Output Port provides data and control signals that permit the gm5020 to connect to a variety of flat panel or CRT devices. The output interface is configurable for 18 or 24-bit RGB pixels, either single or double pixel wide. All display data and timing signals are synchronous with the DCLK output clock.

4.13.1 Display Clock Generation – Display Digital Direct Synthesis Block (DDDS)

The Display DDS is responsible for generating the display clock frequency. The DDDS can operate in two different configurations: Open loop and Closed Loop FRD (Frequency Ratio Detector) method. The implementation of the DDDS is shown in the following diagram:

10 MHz <= DDDS_CLK <= 30 MHz

40 MHz <= Fout <= 330 MHz

10 MHz <= DCLK <= 135 MHz

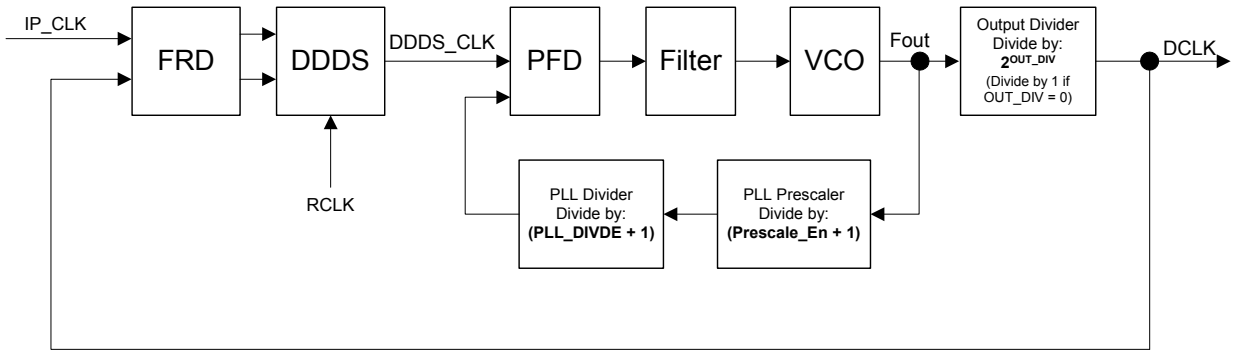


Figure 38. DDDS Block

4.13.1.1. Open Loop Operation

In open loop operation, the display clock (DCLK) is created without consideration to the input clock (IP_CLK in the above diagram). The DDDS acts as a frequency synthesizer with 30-bits of resolution and using RCLK as a reference. By using the DCLK PLL and DCLK output divider, any DCLK frequency between 10 MHz and 135 MHz can be generated.

The DDDS generally operates in this condition to produce valid display timing in the absence of any input. This allows for example, an OSD to be displayed.

4.13.1.2. Closed Loop Operation

In closed loop, the Display DDS creates an optimal display clock frequency by scaling the input clock (from any of analog, digital or video sources). The display clock is scaled using the following relationship:

$$\frac{1}{f(IP\_CLK)} \times SrcHTOTAL \times SrcVTOTAL \times N = \frac{1}{f(DCLK)} \times DispHTOTAL \times DispVTOTAL \times M$$

$$f(DCLK) = f(IP\_CLK) \times \frac{DispHTOTAL \times DispVTOTAL \times M}{SrcHTOTAL \times SrcVTOTAL \times N}$$

Where

f(DCLK) is the frequency of the display clock.

f(IP_CLK) is the frequency of the input clock.

DispHTOTAL is the total number (including blanking) of pixels in the display.

SrcHTOTAL is the total number (including blanking) of pixels in the source.

DispVTOTAL is the total number of lines in the display.

SrcVTOTAL is the total number of lines in the source.

M is the vertical refresh rate of the display.

N is the vertical refresh rate of the source.

In other words by programming the number of display pixels (DispHTOTAL), display lines (DispVTOTAL) and ratio of display frames(M) to source frames(N), the DDDS will synthesize the correct display clock frequency to satisfy the above relationship.

4.13.2 Display Synchronization

The gm5020 supports two display synchronization modes:

- **Free Run Mode:** No synchronization. This mode is used when there is no valid input timing, or for testing purposes.
- **Frame Sync Mode:** The display frame rate is synchronized to the input frame or field rate. This mode is used in most cases – with or without frame rate conversion.

4.13.2.1. Display Free-Run Mode

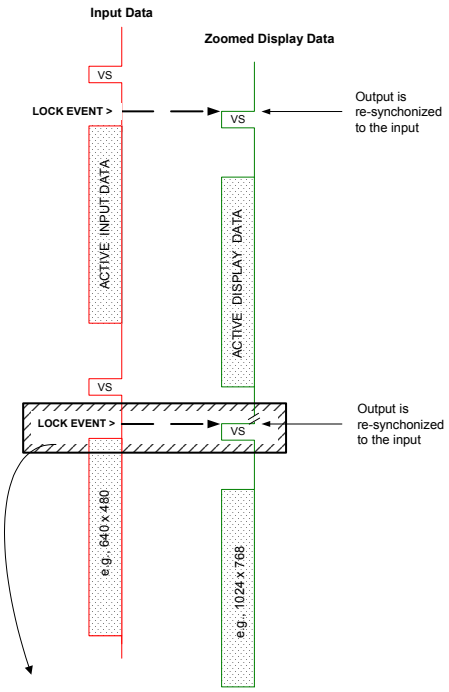
Free-run mode is used when there is no valid input timing (i.e. to display OSD messages or a splash screen). In free-run mode, the display timing is determined only by the values programmed into the display window and timing registers. The DDDS is programmed for open-loop operation and no synchronization is attempted.

4.13.2.2. Frame Sync Mode

Display synchronization is normally done using frame sync mode. In this mode, a 'lock event' (defined in the input timing) determines the frame boundaries in the display timing (display lock load).

Input Lock Event and Display Lock Load

The programmable input Lock Event and display Lock Load parameters represent the mechanism for frame synchronization. The Lock Event represents a chosen pixel location within the input field or frame. When the Lock Event location is reached, the gm5020 Display Timing Generator is reloaded with the Lock Load values. Hence, the display timing is "corrected" or "aligned" to the proper location. This process automatically synchronizes the output to the input, and when properly programmed, prevents gm5020 internal buffer overflow / underflow when no frame buffer is present. The following diagram shows the process when the display frame rate is locked to 1x the input frame rate.



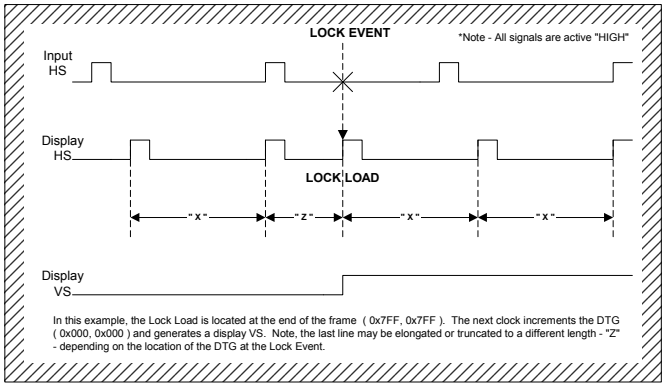


Figure 39. Lock Event Timing (Frame Sync Mode)

Using Frame Sync Mode With and Without Frame Rate Conversion

When frame rate conversion is not being performed, display frames can be synchronized with input frames once every input frame.

When frame rate conversion is being performed, the display is synchronized to the input every 'N' input fields/frames, where 'N' is an integer. For example, if converting from XGA 75Hz to XGA 60Hz (5/4 input/output ratio), synchronization should occur every five input frames.

Note: The Genesis Microchip standard firmware provides a formula to determine the optimum Lock Event location.

4.13.2.3. Manual Synchronization

The gm5020 Display Timing Generator (DTG) may be forced to the lock load values by asserting the DFSYNCn pin. This may be thought of as a "manual" lock event. This manual mechanism is separately enabled via a host register bit. This feature is provided by complex configurations such as slaving gm5020 timing to other devices.

4.13.3 Display Port Timing

Display timing signals provide timing information so the Display Port can be connected to an external display device. Based on values programmed in registers, the Display Output Port produces the horizontal sync (DHS), vertical sync (DVS), and data enable (DEN) control signals. The figure below provides the registers that define the output display timing.

Horizontal values are programmed in single pixel increments relative to the leading edge of the horizontal sync signal. Vertical values are programmed in line increments relative to the leading edge of the vertical sync signal.

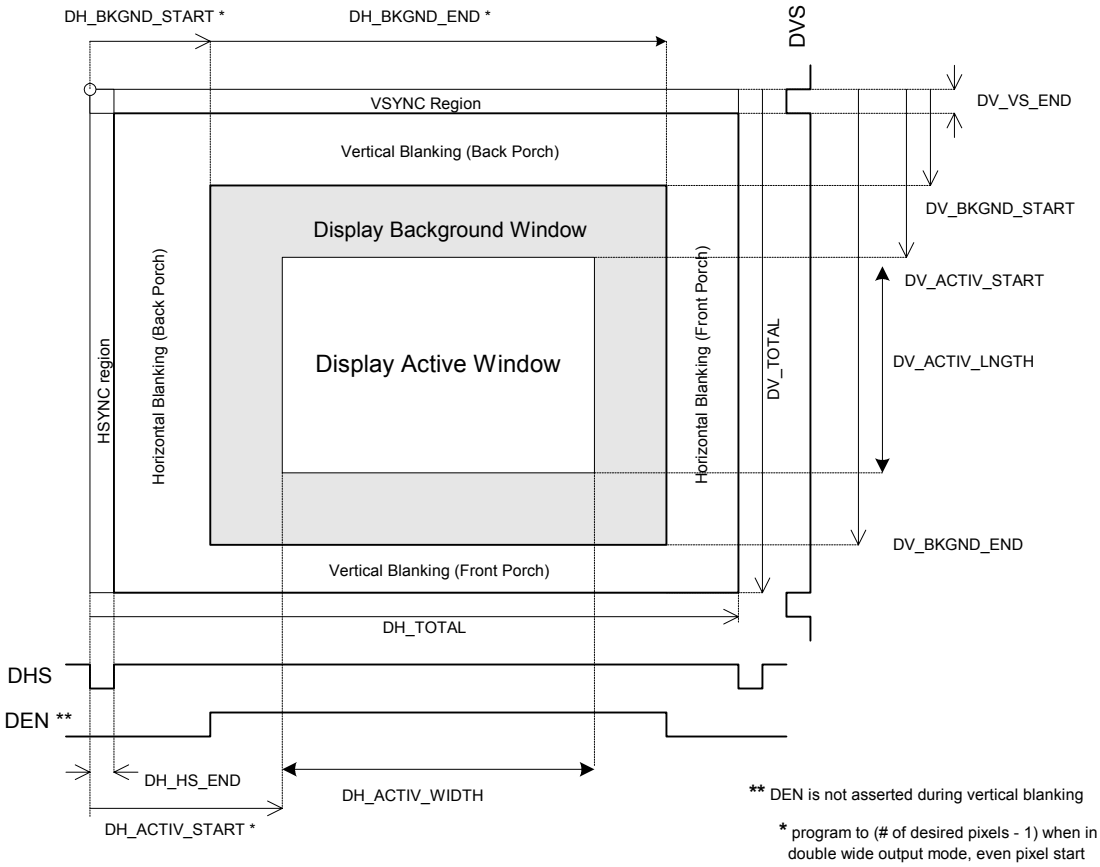


Figure 40. Display Windows and Timing

The display data may be produced either in a single-wide or double-wide format. The double-wide output requires an even number of horizontal pixels to be programmed.

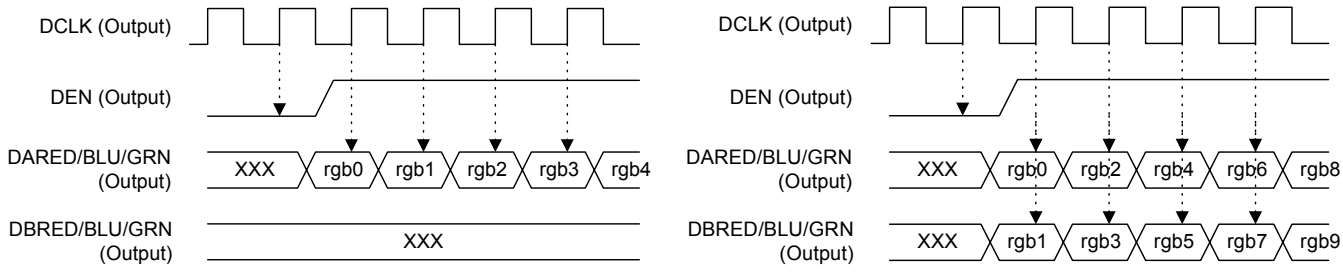


Figure 41. Single / Double-wide Display Data

4.14 Data Path Bypass Options

The gm5020 has three available bypass capabilities in addition to the standard data flow:

1) Capture-only Mode: In this mode, captured input signals and data are transferred, with a nominal register latency, directly to the display output port. No image processing of any type is performed and the display clock is identical to the input clock. The output port is automatically configured for single-pixel data width in this configuration.

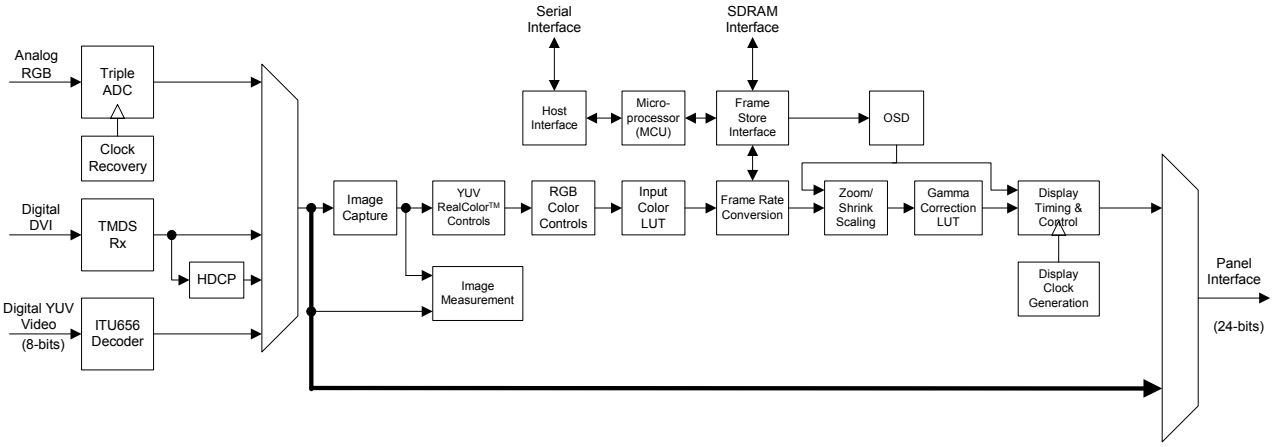


Figure 42. Capture Only Mode

2) FRC Bypass Mode: In this mode, the IC operates without external SDRAM memory. The resultant display vertical sync frequency becomes identical to the input vertical sync frequency (no frame rate conversion). This is the standard operating mode for mid-range SXGA monitors without frame store memory.

Note: Although the external FSCLK pin will not show any activity, the Frame Store Clock must still be active and operating to clock circuitry within the gm5020.

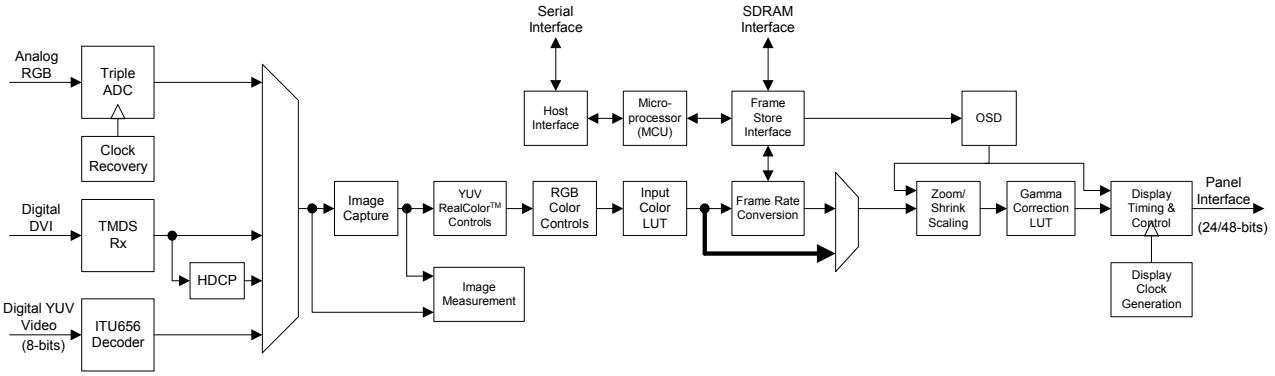


Figure 43. FRC Bypass Mode

3) Scaler Bypass Mode: In this mode, the zoom scaler is bypassed. This mode may be used when the output image resolution is equal to the input image resolution.

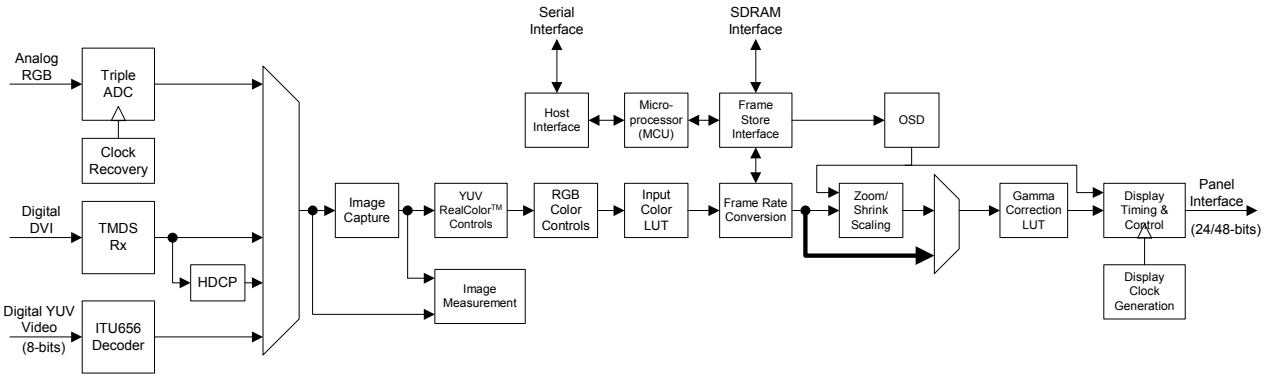


Figure 44. Scaler Bypass Mode

4.15 OSD

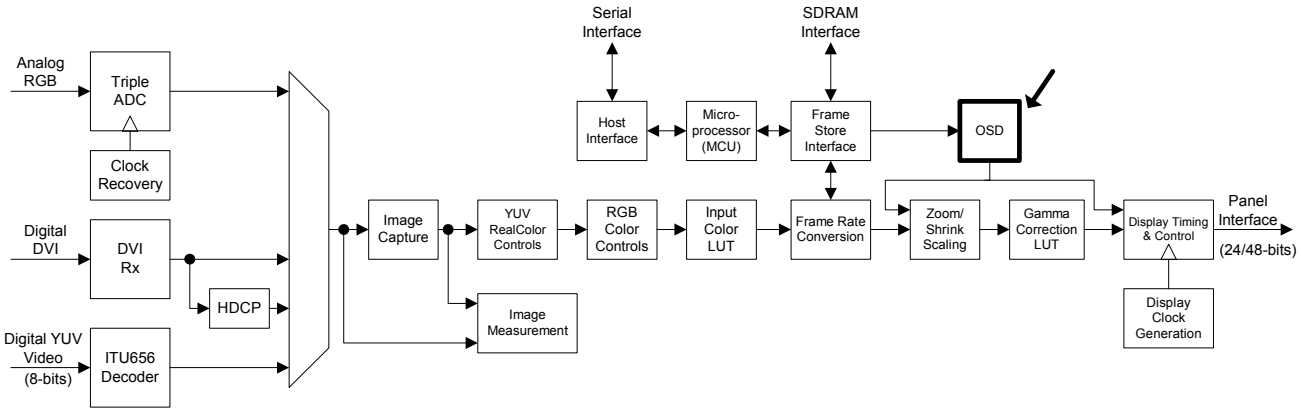


Figure 45. OSD Block

The gm5020 OSD controller supports both character-mapped and bitmapped modes. A user programmable palette of 256 true colors (255 colors, + 1 transparent) is available.

In character mapped mode, a maximum of four colors per character are available.

In 8-bit bitmapped mode, any pixel can be assigned any one of 256 user-defined true colors. In 4-bit bitmapped mode, any pixel can be assigned any one of 16 user-defined true colors (15 colors plus one transparent).

4.15.1 Character Mapped OSD

User-Definable Font Characteristics

Font Location	Font Type	Max Number of Font Colors	Max Character Size in Pixels (horz x vert)	Definable Characters per Table	Max Number of Font Tables
Resident (SRAM)	1-bit / pixel	1 + background	12 x 18	256	1
	1-bit / pixel 90^0 rotated	1+ background	16 x 12	192	1
	2-bits / pixel	3 + background	12 x 18	128< # <=256	1
External (SDRAM)	1-bit/pixel	1+ background	16 x 24	256	4 (+ 1 SRAM) *
	1-bit/pixel 90^0 rotated	1+ background	24 x 16	256	4 (+ 1 SRAM) *
	2-bits / pixel	3+ background	16 x 24	256	4 (+ 1 SRAM) *
	2-bits / pixel 90^0 rotated	3+ background	24 x 16	256	4 (+ 1 SRAM) *

* may be switched on a from row-by-row basis, must be same sized tables

Character Mapped OSD Features:

- Vertical and/or horizontal magnification of OSD image
- Maximum OSD size: 50 characters horizontal x 20 vertical with full character palette defined
- Background Windows Programming support to define an area in the OSD
- 16 levels of blending - suitable for fade effects
- Support for portrait and landscape OSDs (90^0 rotated fonts)
- Pre and post filter merge of OSD into main graphics channel
- Host update of OSD image while OSD is enabled

4.15.1.1. Character Map and On-chip Font Table

The content of the character map specifies the message generated by the OSD.

The character map for the OSD screen is defined by writing into an on-chip character map SRAM (3594 words by 24 bits) by means of the host interface. This on-chip memory is also used to store programmable font characters, if the fonts are not stored in external frame buffer memory.

In memory, the character map is organized as an array of words, each defining the attributes (which character to display, the foreground and background colors, blinking) of one visible character on the screen (starting from upper left of the visible character array). In addition, there is a row attribute word that appears at the beginning of each row of the array in memory (so that the width of the array in memory is one higher than the width of the visible character array). The format of these words is described below.

Registers CHARMAP_XSZ and CHARMAP_YSZ are used to define the visible area of the OSD image. For example, Figure 46 shows a character map for which CHARMAP_XSZ =25 and CHARMAP_YSZ =10.

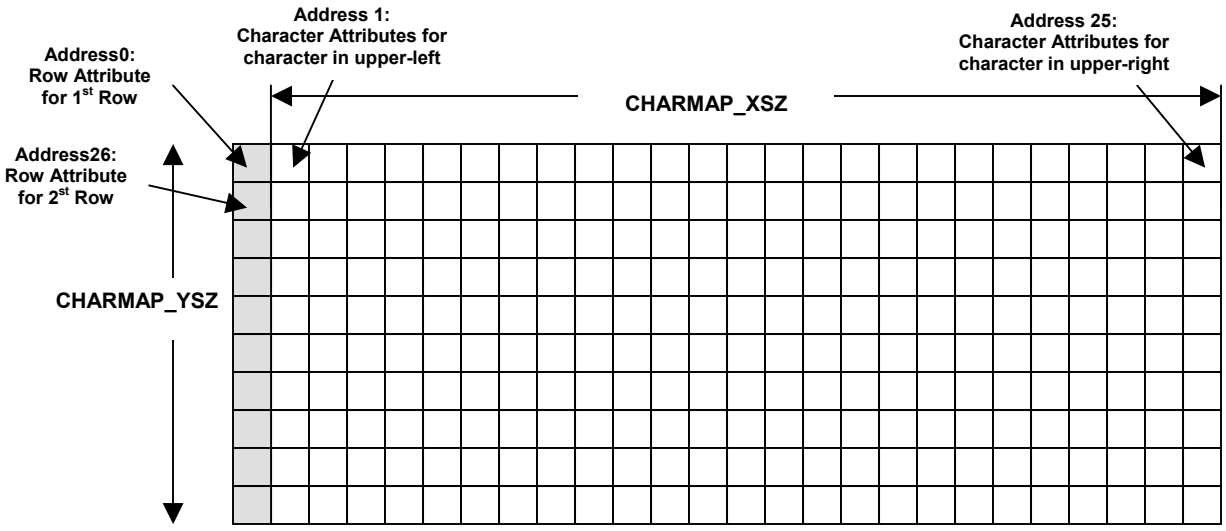


Figure 46. OSD Character Map

Note that when using on-chip programmable fonts, the character map and the font table share the same on-chip RAM. Thus, the size of the character map can be traded off against the number of

fonts. For example, in landscape mode the OSD displayed character screen aspect ratio is programmable and is bounded by the equation:

CHARMAP_XSZ * CHARMAP_YSZ + CHARMAP_YSZ + 18 * ROUND(No. of fonts/2) =< 3594 (one bit per pixel)

(The ROUND operation would round 3.5 to 4.)

CHARMAP_XSZ * CHARMAP_YSZ + CHARMAP_YSZ + 18 * (No. of fonts) =< 3594 (two bits per pixel)

No such restrictions apply when fonts are stored in external frame buffer memory.

Row Attribute Word

The row attribute word at the start of each row in the character array has the following format:

- Bits 23 - 4: Unused
- Bit 3: This bit is used to indicate to the OSD how many colors an SDRAM font uses. If set, the SDRAM font is processed as a two color font. In this mode, the user should use only bit patterns "00" and "11" for describing a font pattern. This mode is useful when WINDOWS BACKGROUND MODE is disabled. SDRAM fonts are processed identically to 1-bit per pixel SRAM fonts – i.e., the SDRAM font will use seven bits (which are independent from the foreground bits) to determine background color.
- Bit 2 [SDRAM_FONT]: If set, characters in this OSD row are retrieved from SDRAM.
- Bit 1 - 0 [SDRAM_FONT_TBL[1:0]]: If SDRAM resident fonts sets are being used, characters in this OSD row use the font table specified by this register.

Character Attribute Word (One bit-per-pixel mode)

In one bit-per-pixel mode, each character attribute word defines the character index, the background color, the foreground color, and the blink status for a visible character.

- Bits 7 - 0: Character Index
- Bits 23 - 16: Bits 7-0 of foreground color (specified by a "1" in the font map)
- Bits 15 - 9: Bits 7-1 of background color (specified by a "0" in the font map) Note that bit 0 of the background color is always "0". Also note that the background color may be defined using the windowing method as described in Section 4.15.1.3 below. In this case these bits are unused.
- Bit 8: A "1" indicates that this character blinks when blinking is enabled.

When only two bit patterns are used to describe an **SDRAM** font ("11" and "00"), bit 3 of the Character Attribute Row can be set, allowing the background color for fonts to be determined by character index bits 7-1. This feature allows a user who is only using two colors in an SDRAM font (11, 00) to choose the background color independent of the foreground color. The foreground and background colors in this case are chosen the same way as a 1-bit per pixel SRAM font; two bits are used to describe two colors because SDRAM fonts must ALWAYS be defined as 2-bits per pixel.
Also note that the background color may be defined using the windowing method as described in Section 4.15.1.3 below. In this case these bits are unused.

Character Attribute Word (Two bit-per-pixel mode)

In two bit-per-pixel mode, each character attribute word defines the character index, the background color, three foreground colors, and the blink status for a visible character.

- Bits 7 - 0: Character Index
- Bits 23 - 20: Bits 7-4 of foreground colors
- Bits 19 - 17: Bits 3-0 of foreground color 3 (pixel bit pattern "11")
- Bits 15 - 12: Bits 3-0 of foreground color 2 (pixel bit pattern "10")
- Bits 11 - 9: Bits 3-1 of foreground color 1 (pixel bit pattern "01")
  Note that bit 0 of foreground color 1 is always "0"
- Bit 8: A "1" indicates that this character blinks when blinking is enabled.

Note that the background color (pixel bit pattern "00") can be defined using the window method as described in section in Section 4.15.1.3 below; alternatively it can be the same as foreground color 2.

Character Map For Rotated OSD

When defining the color and character maps for a rotated OSD image, define the maps from the bottom left hand corner. Note the difference in defining the CHARMAP_XSZ and CHARMAP_YSZ registers for rotated OSD images when compared to non-rotated images.

4.15.1.2. Font Table

Font tables may be defined either in on-chip RAM (same RAM that character map is stored in) or in an external frame buffer. Either way, fonts may be defined using one bit-per-pixel (one foreground color and one background color) or two bits-per-pixel (three foreground colors and one background color).

One Bit Per Pixel On-chip Programmable SRAM Based Fonts

The gm5020 OSD controller has SRAM available to store up to 256, one bit per pixel character mapped fonts. Figure 47 shows the font definition for a character in the on chip SRAM font table, using one bit per pixel protocol. Each font definition is up to 12 pixels horizontal by 18 pixels vertical.

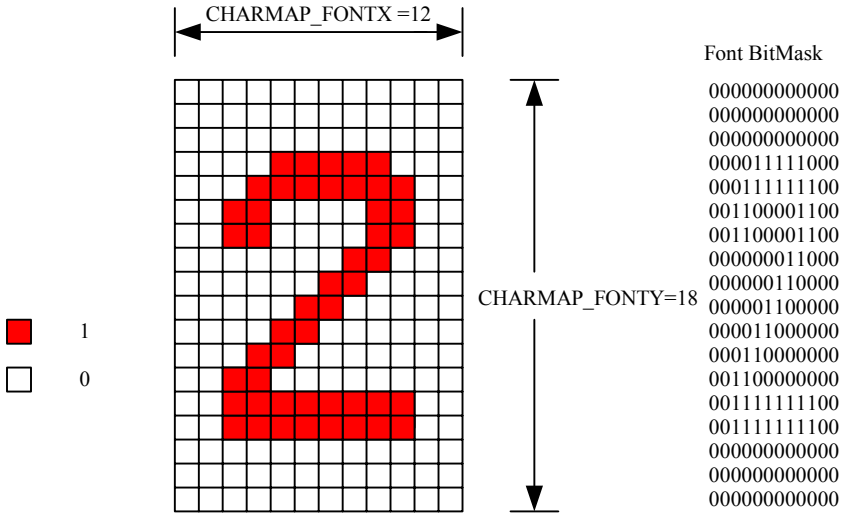


Figure 47. Non-Rotated SRAM Resident Font

Pixels mapped to a “1” are foreground pixels. The foreground index value (FG) programmed into the color index table is then used as the index into the OSD CLUT. Pixels mapped to a “0” are background pixels. The background color for the character is determined by the window region or the background color index value (BG) programmed into the color index table.

Figure 48 shows the font definition for a rotated character in the font SRAM.

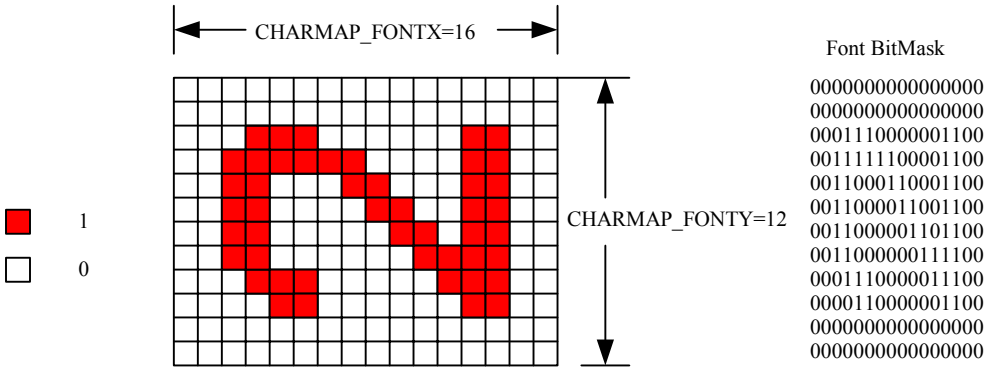


Figure 48. Rotated SRAM Resident Font

Two Bits Per Pixel SRAM Resident Fonts

Typically there is storage space for 128 or more two bit per pixel SRAM resident fonts.

Two bit per pixel SRAM based fonts support up to three foreground colors per character and one background color per character. Figure 49 shows a two bit per pixel SRAM based font definition for a character.

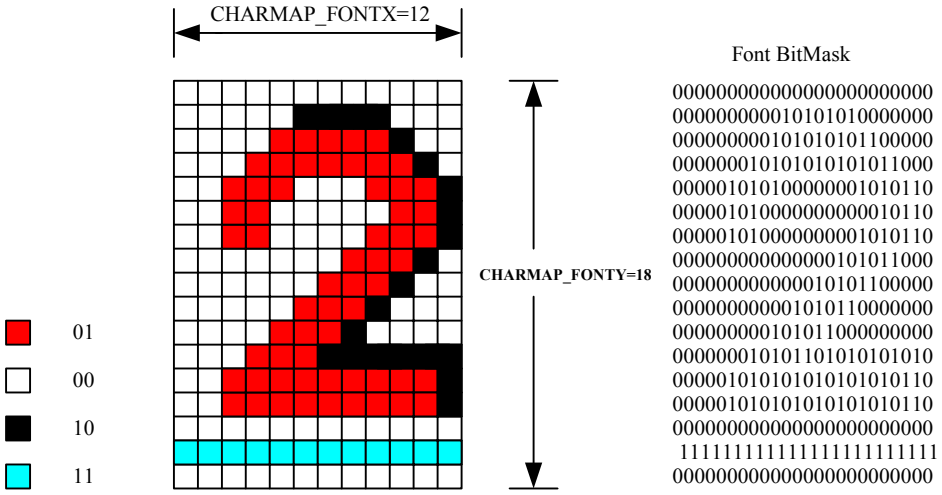


Figure 49. User Define-able SRAM Resident Font

When using 2-bits per pixel SRAM resident fonts, the designer defines each pixel using a 2-bit code. Bit codes “11”, “10”, and “01” are mapped to foreground colors 3, 2 and 1 respectively. Bit

code “00” is mapped to the background color using the window region background color or using foreground color 2.

Frame Buffer Resident Fonts

External frame buffer resident character font tables are supported. The frame buffer interface supplies addresses to fetch character font scan lines via the frame buffer interface port.

The frame buffer based font table supports characters with programmable pixel map organization up to a maximum size of 16 pixels horizontally by 24 pixels vertically. The horizontal character width must be an even number of pixels.

When an external frame buffer is used to store fonts, each character row in the OSD may be programmed to index into one of four user defined font tables. This provides up to 1024 characters in a single character mapped OSD image and is intended to allow multi-language OSD support.

Frame buffer based fonts support up to three foreground colors per character and one background color per character, similar to using two bits per pixel mode using SRAM resident fonts as described above.

4.15.1.3. Background Color of Characters

There are two modes of programming the background color of characters within an OSD image. The OSD controller may be programmed such that it is in Background Windows Mode. This mode of operation allows up to four user programmable background windows to be displayed simultaneously. Each background window has a color attribute, in addition to column and row start and stop parameters. Background Windows Mode enables OSD images to be quickly designed with little programming.

With Background Windows Mode disabled, the background color of characters may be programmed such that each character has a unique background color.

Background Windows Mode Enabled

Up to four background windows are supported. The windows control the background color. Windows may overlap and have a priority sequence. Window sizes are programmable and are defined by host registers. Transparency is achieved by setting the background color for a window to “00”.

Background Windows Mode Disabled

When background windows are disabled, the background color for each character in the OSD image is user-programmable. In one bit per pixel mode each character has one foreground and one background color defined. In two bit per pixel mode each character has three foreground colors defined, and the background color is the same as foreground color 2.

4.15.1.4. Character Blinking

Character blinking is enabled by setting bit 8 of the character attribute. A global host parameter is set to then make the desired characters blink. Blink frequency and duty cycle is programmable through host registers. When a character is blinking, foreground colors periodically revert to the background color of the character. Blinking frequency is proportional to the display frame rate.

4.15.1.5. Character Spacing

The characters within a character mapped OSD image may have additional spacing added between each character definition. See the register specification for allowed spacing. When spacing is added to a character, background color pixels are inserted around the character to achieve the desired spacing. Character spacing is added before horizontal and vertical stretching causing spaces to be stretched along with the character.

4.15.2 Bitmapped OSD

The OSD block supports bitmapped images stored in SDRAM.

The bitmap is loaded into the external frame buffer by the host. The OSD block fetches the bitmap from the frame buffer and uses the data to define the displayed pixel colors on a pixel by pixel basis. Pixels can be represented using either 8 bits per pixel (256 simultaneous colors) 4 bits per pixel (16 simultaneous colors with lower SDRAM requirement), 2 bits per pixel (4 colors) or 1 bit per pixel.

The maximum bitmapped image size is 512 horizontal x 512 pixels vertical.

4.15.3 Color Look-up Table (LUT)

Each pixel of a displayed character is resolved to an 8-bit color code. This selected color code is then transformed to a 24-bit value using a 256 x 24-bit look up table. Color index value “00” is reserved for transparent OSD pixels. The LUT is stored in an on-chip SRAM and is loaded via the Host interface.

4.15.4 Multiple OSD Windows

Up to three OSDs may appear on the screen at any given time: two bitmapped OSDs and one character-mapped OSD.

4.15.5 OSD Stretch

The OSD image can be stretched horizontally and/or vertically by a factor of two, three, or four. Pixel and line replication is used to stretch the image.

4.15.6 Blending

16 levels of blending are supported for the character-mapped and bitmapped images. One host register controls the blend levels for pixels with LUT values of 128 and greater, while another host register controls the blend levels for pixels with LUT values of 127 and lower. OSD color LUT value 0 is reserved for transparency and is unaffected by the blend attribute.

Blend levels for binary codes “1111” through “0000” are 6.25%, 12.5%, 18.75%, 25%, 31.25%, 37.5%, 43.75%, 50%, 56.25%, 62.5%, 68.75%, 75%, 81.25%, 87.5%, 93.75%, 100%. Blend percentage level refers the percentage of the output data that is OSD. For example, 0001 yields an output data stream whose blended pixel data is 93.75% OSD and 6.25% underlying image data. This OSD would be only slightly translucent.

4.15.7 OSD Merge

The OSD data can be merged before or after the scaling engine. Character mapped image would typically be merged after the scaling engine. Merge location is common for all OSD images (bitmapped and character mapped) at any given time.

4.16 On-Chip Microprocessor

The gm5020 incorporates an embedded microprocessor, or OCM (On-Chip Microprocessor). This processor is intended to simplify the gm5020 system software implementation by providing embedded macro functions such as complex OSD menu configurations (bitmapped or proportional fonts). It is not intended to replace the system microprocessor.

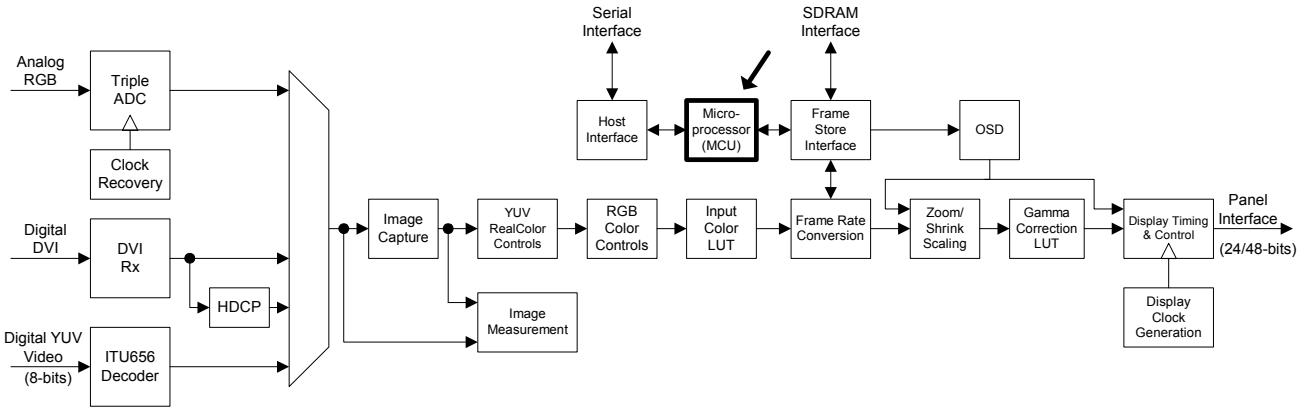


Figure 50. MCU Block

An arbitration mechanism handles the register access requests from the OCM and the system microcontroller.

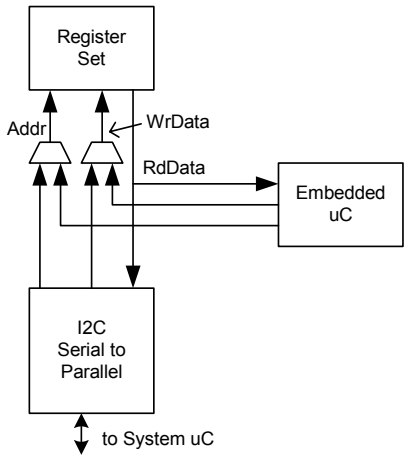


Figure 51. System µC - Embedded µC Communication

4.17 Bootstrap Configuration

During hardware reset, the frame store address lines (FSADDR [13:0]) are configured as inputs. On the de-assertion of reset (rising edge of RESETn), the value on the address lines is captured by the gm5020. The designer should install a 10K pull-up resistor to indicate a '1'and connect to ground to indicate a '0'. The captured values are latched into readable host registers. The value on FSADDR [6:0] specifies the 2-wire host protocol device address.

Note: All bootstrap pins must be connected to a known logic voltage and NOT be left floating.

Table 14. Bootstrap Signals

Name	I/O	Shared With	Description
ADDR(6:0)	I	FSADDR(6:0)	If using 2-wire protocol, this determines the chip address.
USER_BITS(4:0)	I	FSADDR(4:0)	If using 6-wire nibble protocol, these settings are available for reading from a status register for any general-purpose user function. They are otherwise unused by the IC.
Reserved	I	FSADDR5	If using 6-wire nibble protocol, bootstrap this bit to 0.
Reserved	I	FSADDR6	If using 6-wire nibble protocol, bootstrap this bit to 0.
HOST_PROTOCOL	I	FSADDR7	Selects the host interface protocol 0 = 2-wire protocol 1 = 6-wire (nibble) protocol (recommended)
USER_BITS(7:5)	I	FSADDR(10:8)	These settings are available for reading from a status register for any general-purpose user function. They are otherwise unused by the IC
OCM_START	I	FSADDR11	Set to '0'
OCM_CLK	I	FSADDR13:12	Select over-sampling clock source for Host Interface and OCM. 00 = RCLK PLL / 2 10 = TCLK 00, 01 = EXTCLK

4.18 Host Interface

The purpose of the host interface is to connect to the external system microcontroller (MCU). The gm5020's host microcontroller interface has two modes of operation: 2-Wire compatible mode, and a 6-wire (nibble wide) interface mode, which are selected by bootstrapping options.

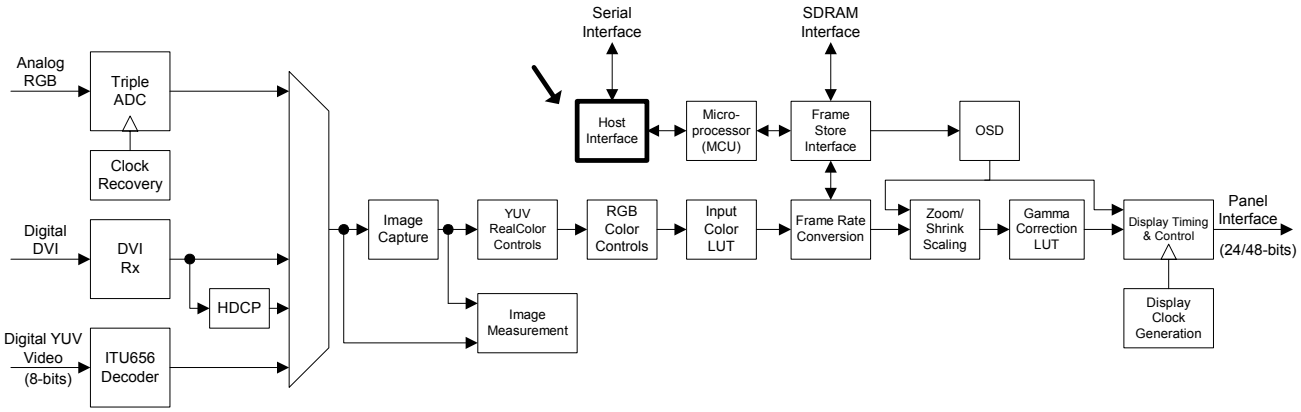


Figure 52. Host Interface Block

4.18.1 2-wire Configuration

The 2-wire compatible connection consists of a serial clock (SCL) and bi-directional serial data line (SDA). The bus master drives the SCL clock and either the master or slave may drive the SDA line (open drain). The gm5020 operates as a slave on the interface and the external MCU as the master. The SDA and SCL lines are shared with the 6-wire communication lines HFSn and HCLK respectively, as illustrated below.

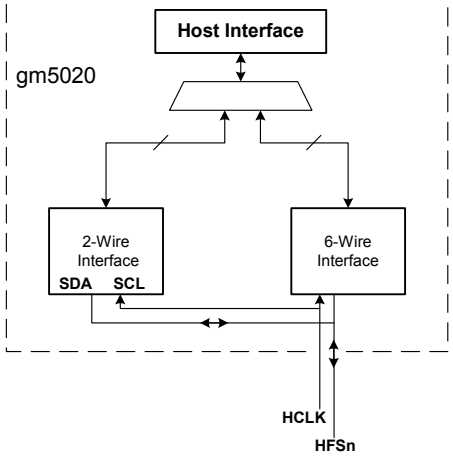


Figure 53. 2-Wire External Interface

The 2-Wire protocol requires a 7-bit device identification address. 2-Wire mode is selected by boot-stapping HOST_PROTOCOL (FSADDR7) to "0" and providing the device identification address on FSADDR[6:0]) on the rising edge of RESETn.

4.18.1.1. Host Interface Command Format

Transactions on the 2-wire host protocol occurs in integer multiples of bytes (i.e. 8 bits or two nibbles respectively). These form an instruction byte (described in Table 15), a device register address and/or one or more data bytes.

The first byte of each transfer indicates the type of operation to be performed by the gm5020. The table below lists the instruction codes and the type of transfer operation. The content of bytes that follow the instruction byte will vary depending on the instruction chosen. By utilizing these modes effectively, registers can be quickly configured.

The LSB of the instruction code, denoted 'A8' in Table 15 below, is bit 8 of the internal register address respectively. It is set to '0' to select a starting register address of less than 256 (0x00 through 0xFF), or '1' to select an address greater than 255 (0x100 through 0x1FF). This bit of the address increments in Address Increment transfers. The unused bits in the instruction byte should be set to '1'.

Table 15. Instruction Byte Map

Value 7 6 5 4 3 2 1 0	Operation Mode	Description
0 0 0 1 x x x A8	Write Address Increment	Allows the user to write a single or multiple bytes to a specified starting address location. A Macro operation will cause the internal address pointer to increment after each byte transmission. Termination of the transfer will cause the address pointer to increment to the next address location.
0 0 1 0 x x x A8	Write Address No Increment (for table loading)	
1 0 0 1 x x x A8	Read Address Increment	Allows the user to read multiple bytes from a specified starting address location. A Macro operation will cause the internal address pointer to increment after each read byte. Termination of the transfer will cause the address pointer to increment to the next address location.
1 0 1 0 x x x A8	Read Address No Increment (for table reading)	
0 0 1 1 x x x A8 0 1 0 0 x x x A8 1 0 0 0 x x x A8 1 0 1 1 x x x A8 1 1 0 0 x x x A8	Reserved	
0 0 0 0 x x x A8 0 1 0 1 x x x A8 0 1 1 0 x x x A8 0 1 1 1 x x x A8 1 1 0 1 x x x A8 1 1 1 0 x x x A8 1 1 1 1 x x x A8	Spare	No operation will be performed

4.18.1.2. Serial Protocol

A data transfer consists of a stream of serially transmitted bytes formatted as shown in the figure below. A transfer is initiated (START) by a high-to-low transition on SDA while SCL is held high. A transfer is terminated by a STOP (a low-to-high transition on SDA while SCL is held high) or by a START (to begin another transfer). The SDA signal must be stable when SCL is high, it may only change when SCL is low (to avoid being misinterpreted as START or STOP).

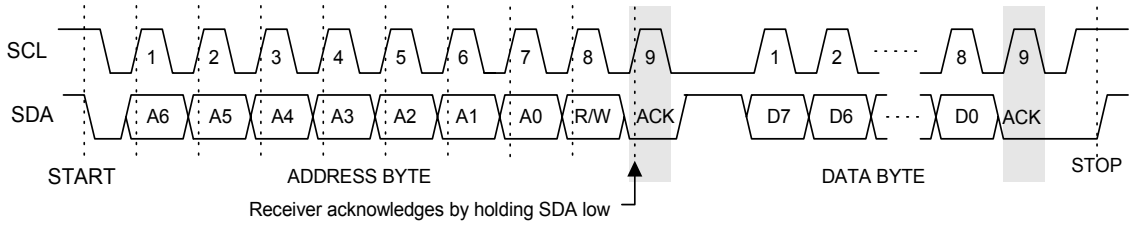


Figure 54. 2-wire Protocol Data Transfer

Each transaction on the SDA is in integer multiples of bytes (8 bits). The number of bytes that can be transmitted per transfer is unrestricted. Each byte is transmitted with the most significant bit (MSB) first. After the eight data bits, the master releases the SDA line and the receiver asserts the SDA line low to acknowledge receipt of the data. The master device generates the SCL pulse during the acknowledge cycle. The addressed receiver is obliged to acknowledge each byte that has been received.

Write Address Increment and Write Address No Increment

The Write Address Increment and the Write Address No Increment mode of operation allows one or multiple registers to be programmed with only sending one start address. In Write Address Increment, the address pointer is automatically incremented after each byte has been sent and written. The transmission data stream for this mode is illustrated below. The highlighted sections of the waveform represent moments when the transmitting device must release the SDA line and wait for an acknowledgement from the gm5020 (the slave receiver).

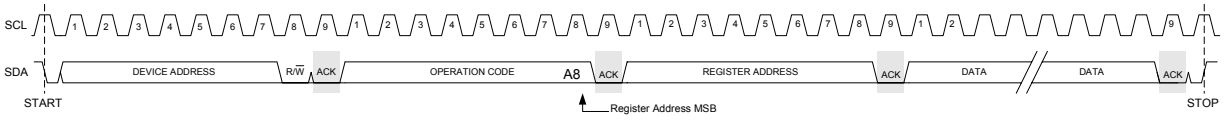


Figure 55. Write Address Increment and Write Address No Inc (0x10 & 0x20)

Read Address Increment and Read Address No Increment

The Read Address Increment and the Read Address No Increment mode of operation allows one or multiple registers to be read with only sending one start address. In Address Read Increment, the address pointer is automatically incremented after each byte has been sent. The transmission protocol for this mode is illustrated below. The highlighted sections of the waveform represent

moments when the transmitting device must release the SDA line and waits for an acknowledgement from the master receiver.

Note that on the last byte read, no acknowledgement is issued to terminate the transfer.

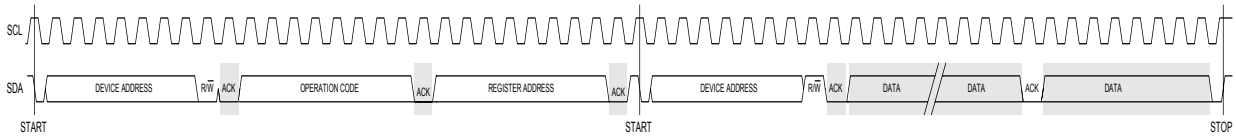


Figure 56. Read Address Increment and Read Address No Inc (0x90 & 0xA0)

Direct Read

It is also possible to perform a read as illustrated below. The internal address will only increment after each byte if the previous operation code was an incremented operation, i.e., the previous operation state is retained.

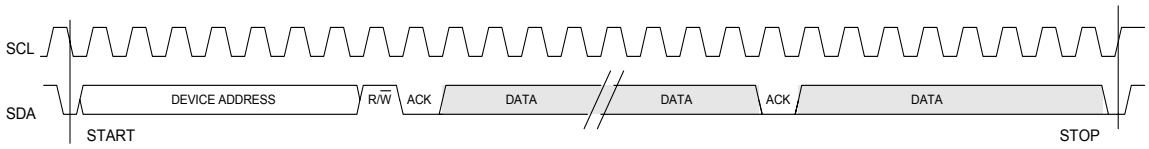


Figure 57. Direct Read

4.18.2 6-Wire Configuration

The 6-wire interface connection features four bi-directional data lines HDATA[3:0], one clock (HCLK), and one chip select / framing signal (HFSn). Four bits are transferred on each clock edge. The gm5020 operates as a slave on the interface with the external MCU expected to generate HCLK.

This configuration provides the maximum transfer rate, operating up to 1/20th the selected internal OCM_CLK. The OCM_CLK typically operates at 100MHz, thus allowing a HCLK frequency of 5 MHz. This presents a maximum 20 Mbit/second data transfer. This configuration is strongly recommended for complex OSDs or multiple font sets.

Protocol selection is performed during power-up at the rising edge of RESETn input. The 6-Wire protocol is selected via a bootstrap configuration (HOST_PROTOCOL (FSADDR7) = “1”.)

HFSn

The host framing signal is a master enable for the host interface. If HFSn is de-asserted (high), then all activity on the remaining signals shall be ignored. If the HFSn is asserted (low), the host interface responds to bus activity. The assertion of HFSn marks the START condition upon which the host interface is initialized, and the de-assertion of HFSn marks the end condition upon which all pending operations are cleared.

HCLK

HCLK is the clock by which data is loaded into, or read from the host interface. HCLK is active low; the gm5020 captures on the falling edge and transmits on the rising edge of HCLK.

HDATA[3:0]

HDATA[3:0] contains the data that is written to, and read from the host interface. This is a bi-directional data bus, and thus must be tri-stated by the master device whenever reading from the gm5020. Each line on this bi-directional bus requires a pull-up resistor.

The serial interface port operates as a slave device and is uniquely addressed by the HFSn input. The HFSn signal must be de-asserted during a Hardware Reset (i.e. when RESETn is asserted). A master device initiates a data transfer by asserting HFSn (START) and terminated by de-asserting HFSn (STOP). HCLK must be inactive for no less than ½ HCLK cycle before HFSn is asserted and after HFSn is de-asserting. The HFSn signal must be de-asserted for a minimum of a half cycle between transfers.

A data transfer consists of a number of sequentially transmitted bytes, sent four bits at a time on HDATA[3:0], formatted as shown in the figures below. Bytes are transferred on the HDATA lines with the most significant bit (MSB) first. The number of bytes that can be transmitted per transfer is unrestricted. The protocol supports static operation, and can be halted or started by controlling the HCLK at any time during a transfer.

4.18.2.1. Command Format

The data transfers using the 6-Wire protocol consist of an instruction byte indicating the type of operation to be performed by the gm5020. Table 15 above lists the instruction codes and the type of transfer operation. The content of bytes that follow the instruction byte will vary depending on the instruction chosen.. All operation modes and instruction codes are identical to those of the 2-Wire protocol. See Section 4.18.1. No data acknowledge is implemented in the 6-Wire protocol. It is the responsibility of the external controller to verify, via transfer operations, that data is received and transmitted correctly.

4.18.2.2. 6-Wire Protocol

The data transfer formats following the instruction byte are identical to 2-wire with the following exceptions:

- The HFSn signal is used for direct addressing, therefore no device address byte is sent. The first byte instead contains the instruction byte indicating the type of operation to be performed. Figure 58 shows and equivalent Write Address Increment operation. (‘Increment’ Write implies that the register address is incremented after each data byte is read or written, allowing the user to program a block of sequential addresses, stating only a single starting address.)

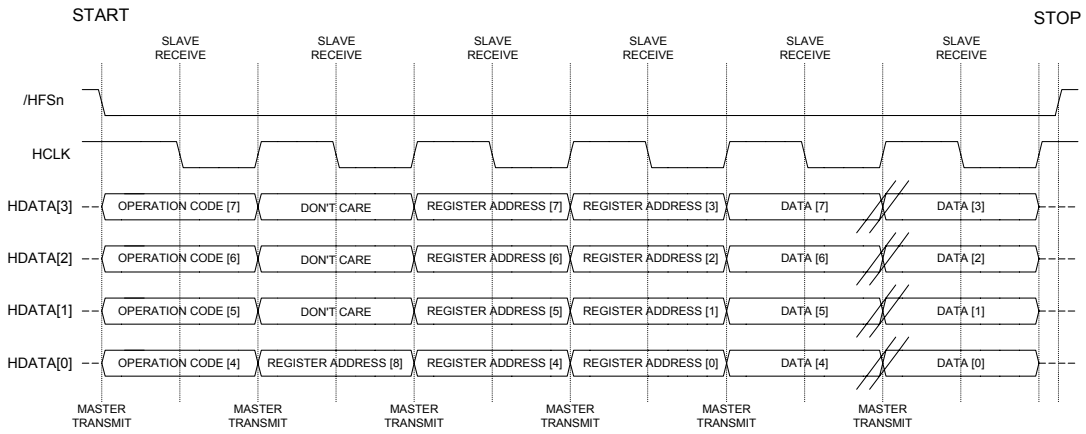


Figure 58. 6-Wire Write Operations (0x1*x* & 0x2*x*)

- Read operations can be performed in one transfer without a re-start cycle and re-send of the device address before data is sent from the slave device. Data is sent in the byte immediately following the instruction or address. Figure 59 shows the equivalent operation for the Read Address Increment transfer.

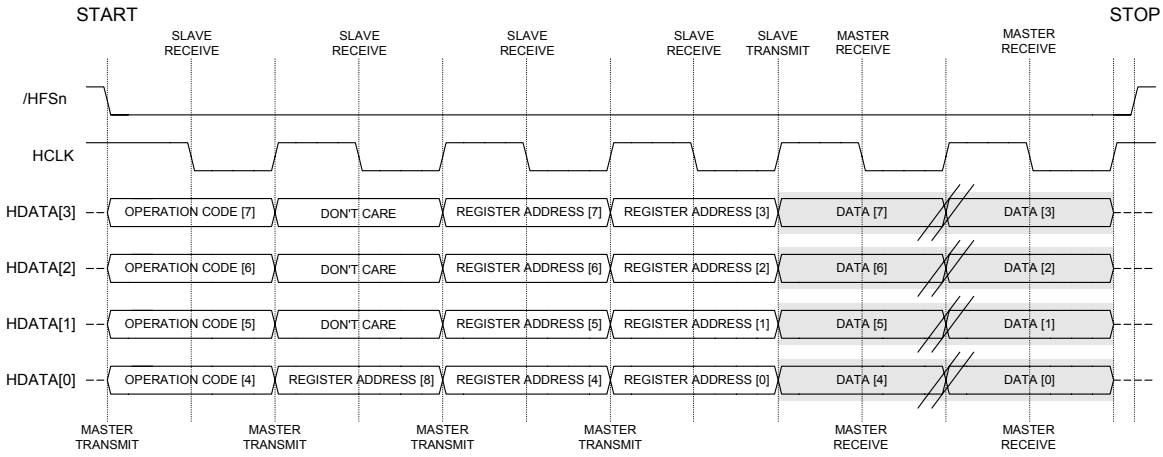


Figure 59. 6-Wire Read Operations (0x9*x* & 0xA*x*)

4.19 Miscellaneous Functions

4.19.1 General Purpose Inputs and Outputs (GPIO's)

The gm5020 has nine general purpose inputs / outputs. These are typically used to communicate with other devices in the system such as keypad buttons, NVRAM, LEDs, audio DAC, etc. Each GPIO has independent direction control as well as open drain or active drive selection.

GPIO0 and GPIO1 may be optionally configured as PWM back light intensity controls, as described in section 4.19.2 below.

In addition to these nine GPIOs, the video port data pins (YUV 7:0) can also serve as general-purpose inputs. YUV 7:0 are available to be directly read from the host register – there is no directional control required.

4.19.2 Pulse Width Modulation (PWM) Back Light Control

Many of today's LCD back light inverters require both a PWM input and variable DC voltage to minimize flickering (due to the interference between panel timing and inverter's AC timing), and adjust brightness. Many LCD monitor designs currently use a microcontroller to provide these control signals. To minimize the burden and required resources of the external microcontroller, the gm5020 generates these signals directly.

There are two pins available for controlling the back light of TFT LCD panels, PWM0 (GPIO0) and PWM1 (GPIO1). The duty cycle of these signals is programmable. They may be connected to an external RC integrator to generate a variable DC voltage for a LCD back light inverter. The display HSYNC signal (DHS) or TCLK may be used as the clock for a counter generating this output signal.

4.19.3 Low Power State

The gm5020 provides a low power state in which the clocks to selected parts of the chip may be disabled. See Table 17.

5. ELECTRICAL SPECIFICATIONS

5.1 DC Characteristics

Table 16. Absolute Maximum Ratings (Both gm5020 and gm5020-H)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage AVDD_3.3 & DVDD_3.3 & PLLVDD_3.3	V_{VDD_33}	-0.3		3.6	V
Supply Voltage AVDD_2.5 & DVDD_2.5	V_{VDD_25}	-0.3		2.75	V
Input Voltage (5V tolerant inputs)	V_{IN}	-0.3		5.5	V
Input Voltage (non 5V tolerant inputs)	V_{IN}	-0.3		3.6	V
Electrostatic Discharge	V_{ESD}			±2.0	kV
Latchup	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	°C
Storage Temperature	T_{STG}	-40		125	°C
Operating Junction Temp.	T_J	0		125	°C
Case Temperature	T_C			125	°C
Thermal Resistance: (Junction to Ambient) Natural Convection	θ_{JA}			18.0	°C/W
Thermal Resistance: (Junction to Case) Convection or air flow	θ_{JC}			6.9	°C/W
Soldering Temperature (30 sec.)	T_{SOL}			220	°C
Vapor Phase Soldering (30 sec.)	T_{VAP}			220	°C

NOTE 1: All voltages are measured with respect to GND.

NOTE 2: Absolute maximum voltage ranges are for transient voltage excursions.

NOTE 3: Package thermal resistance is based on a PCB with one signal and two power planes. Package θ_{JA} is improved with four or more layer PCB.

Table 17. DC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage AVDD_3.3 / DVDD_3.3 / PLLVDD_3.3	V_{VDD_33}	3.15	3.3	3.45	V
Supply Voltage AVDD_2.5 / DVDD_2.5	V_{VDD_25}	2.35	2.5	2.65	V
Power Consumption: (1)					
UXGA 60Hz source to SXGA 60Hz display	P_{SXGA}		1.75	2.6	W
SXGA 85Hz source to XGA 60Hz display	P_{XGA}		1.55	2.0	W
Low Power Mode(2)	P_{LP}		0.5		W
Supply Current: (3)					mA
UXGA 60Hz source to SXGA 60Hz display					
• 2.5V digital supply	$I_{SXGA\_25\_VDD}$		440	575	
• 2.5V analog supply	$I_{SXGA\_25\_AVDD}$		40	45	
• 3.3V digital supply	$I_{SXGA\_33\_VDD}$		70	190	
• 3.3V analog supply	$I_{SXGA\_33\_AVDD}$		80	110	
• 3.3V PLL supply	$I_{SXGA\_33\_PLL}$		20	30	
SXGA 85Hz source to XGA 60Hz display					
• 2.5V digital supply	$I_{XGA\_25\_VDD}$		410	510	
• 2.5V analog supply	$I_{XGA\_25\_AVDD}$		40	45	
• 3.3V digital supply	$I_{XGA\_33\_VDD}$		60	115	
• 3.3V analog supply	$I_{XGA\_33\_AVDD}$		80	110	
• 3.3V PLL supply	$I_{XGA\_33\_PLL}$		20	30	
INPUTS					
High Voltage	V_{IH}	2.0		V_{DD}	V
Low Voltage	V_{IL}	GND		0.8	V
Clock High Voltage	V_{IHC}	2.4		V_{DD}	V
Clock Low Voltage	V_{ILC}	GND		0.4	V
High Current (V_{IN} = 5.0 V)	I_{IH}	-25		25	µA
Low Current (V_{IN} = 0.8 V)	I_{IL}	-25		25	µA
Capacitance (V_{IN} = 2.4 V)	C_{IN}			8	pF
OUTPUTS					
High Voltage (I_{OH} = Pin drive strength**)	V_{OH}	2.4		V_{DD}	V
Low Voltage (I_{OL} = Pin drive strength**)	V_{OL}	GND		0.4	V
Tri-State Leakage Current	I_{OZ}	-25		25	µA

Note (1): Maximum power conditions are V_{VDD_33} = 3.45V, V_{VDD_25} = 2.65V, Worst-case (high-switching) input image. Typical power conditions are V_{VDD_33} = 3.30V, V_{VDD_25} = 2.50V, Typical (Windows-type) input image.

Note (2): Low power figures result from setting the ADC, DVI, and clock power down bits.

Note (3): Maximum current values are not achieved simultaneously.

5.2 Preliminary AC Characteristics

The following targeted specifications have been derived by simulation. All timing is measured to a 1.5V logic-switching threshold. The minimum and maximum operating conditions used were:

$0°C \leq T_{DIE} \leq 125°C$, $2.35 \leq V_{DD25} \leq 2.65$, $3.15 \leq V_{DD33} \leq 3.45$, $C_{LOAD} = 16$ pF
Process = best to worst

Table 18. Maximum Speed of Operation

Clock Domain	gm5020 / gm5020-H
Main Input Clock (TCLK)	50 MHz (24 MHz recommended)
DVI Clock	165MHz
ADC Clock	162MHz
ITU-R BT656 Clock	75 MHz
SCL Host Interface Clock (2-wire mode)	400kHz
HCLK Host Interface Clock (6-wire mode)	5 MHz
IFM_CLK Input Format Measurement Clock	50MHz
R_CLK Reference Clock	200MHz
F_CLK Frame Store Clock FRC/non-FRC configuration	144 MHz (120 MHz recommended)/ 156 MHz
OCM_CLK On-Chip MCU	100 MHz
DCLK Display Clock	135 MHz

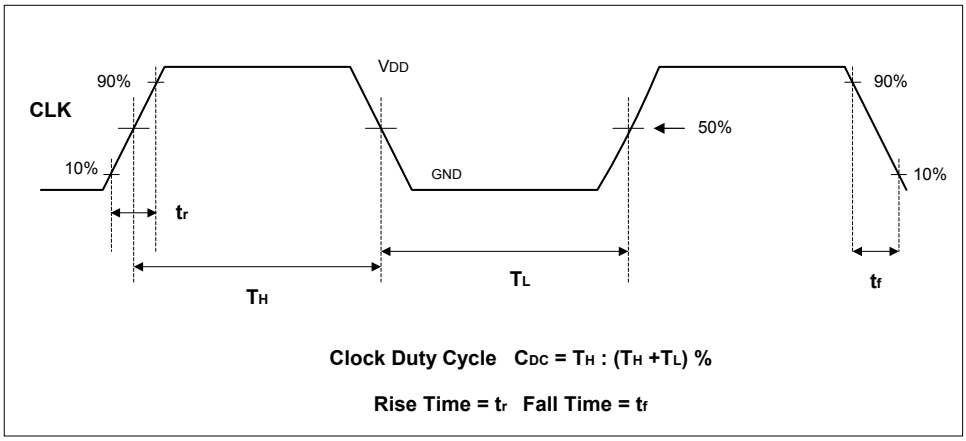


Figure 60. Clock Reference Levels

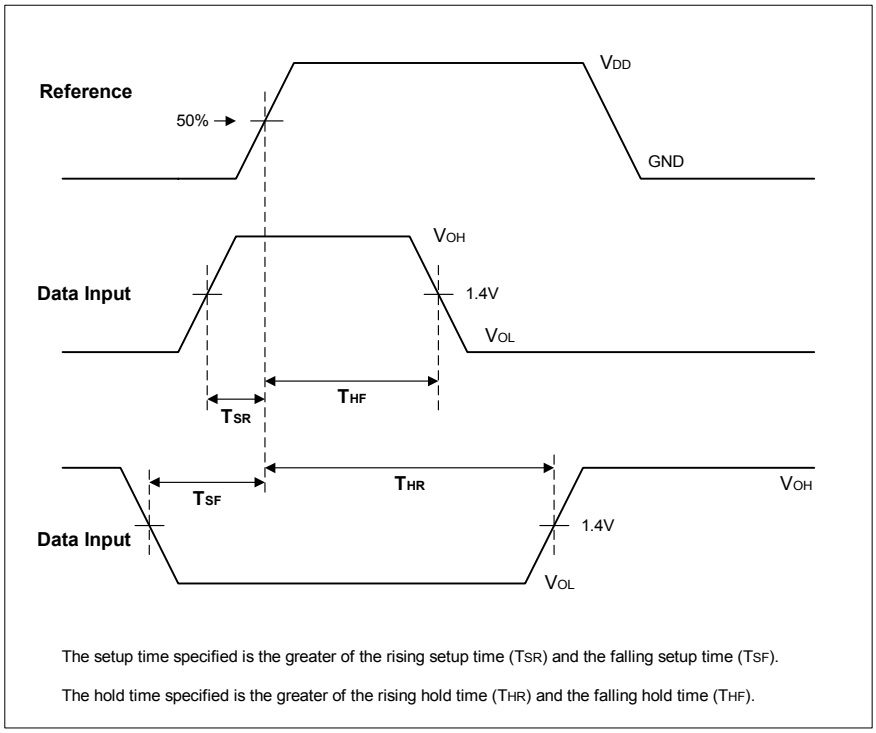


Figure 61. Setup and Hold Reference Levels

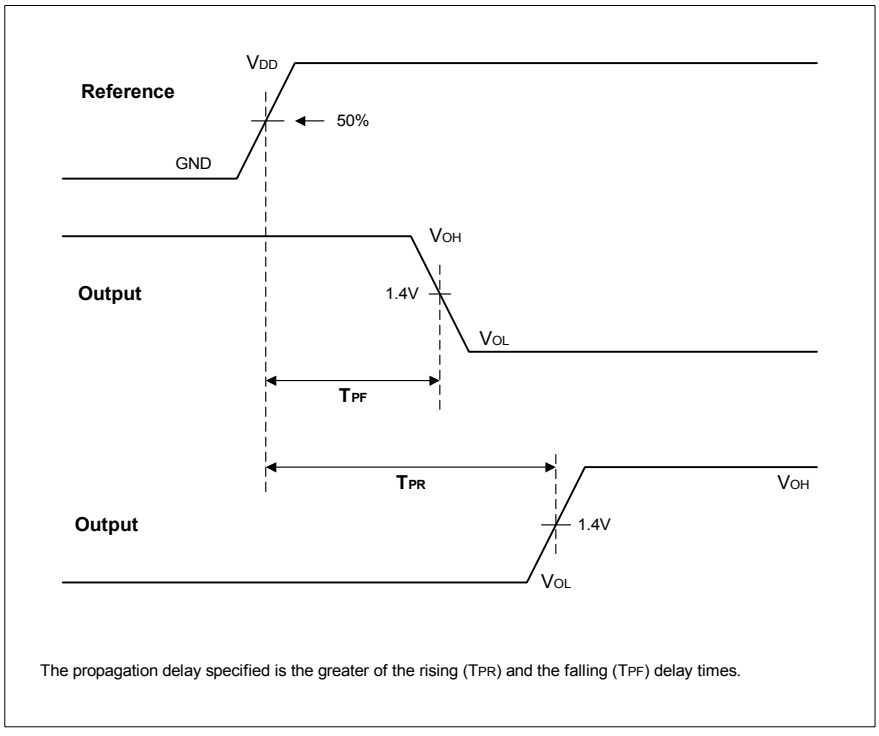


Figure 62. Propagation Delay Reference Levels

Table 19. ITU-R BT656 Input Port Timing

Signal	Minimum Setup Requirement (ns)	Minimum Hold Requirement (ns)
YUV [7:0]	4.0	1.0

Table 20. Framestore Output Timing and Adjustments

FSOUT_TIMING ->	Tap 0 (default)		Tap 1		Tap 2		Tap 3	
	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Propagation delay from FSCLK to FSDATA* (output)	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5
Propagation delay from FSCLK to FSADDR*	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5
Propagation delay from FSCLK to FSRAS	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5
Propagation delay from FSCLK to FSCAS	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5
Propagation delay from FSCLK to FSWE	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5
Propagation delay from FSCLK to FSDQM1	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5
Propagation delay from FSCLK to FSDQM0	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5
Propagation delay from FSCLK to FSCKE	1.0	4.5	0.5	3.5	0.0	2.5	-0.5	1.5

Note: This table lists the amount of adjustment that can be made to the framestore output propagation delays, in order to improve setup margin of DRAM write operations at the expense of Hold margin on write operations and setup margin on read operations. The tap selected is controlled by the FSOUTTIMING parameter in the SYS_TIMING register.

Table 21. Framestore Readback Timing (for all conditions)

FSREAD_TIMING Tap 0	FSOUTTIMING			
	Tap 0	Tap 1	Tap 2	Tap 3
FSDATA* Minimum Setup (ns)	2.5	3.5	4.5	5.5
FSDATA* Minimum Hold (ns)	1.0	0.5	0.0	-0.5

FSREAD_TIMING Tap 1	FSOUTTIMING			
	Tap 0	Tap 1	Tap 2	Tap 3
FSDATA* Minimum Setup (ns)	0.5	1.5	2.5	3.5
FSDATA* Minimum Hold (ns)	2.0	1.5	1.0	0.5

FSREAD_TIMING Tap 2	FSOUTTIMING			
	Tap 0	Tap 1	Tap 2	Tap 3
FSDATA* Minimum Setup (ns)	1.5	2.5	3.5	4.5
FSDATA* Minimum Hold (ns)	1.5	1.0	0.5	0.0

FSREAD_TIMING Tap 3	FSOUTTIMING			
	Tap 0	Tap 1	Tap 2	Tap 3
FSDATA* Minimum Setup (ns)	3.0	4.0	5.0	6.0
FSDATA* Minimum Hold (ns)	0.5	0.0	-0.5	-1.0

Note: FSOUTTIMING and FSREADTIMING are controlled by the SYS_TIMING register.

Table 22. Display Timing and DCLK Adjustments

DP_TIMING ->	Tap 0 (default)		Tap 1		Tap 2		Tap 3	
	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Propagation delay from DCLK to DA*/DB*	1.0	4.5	0.5	3.5	-0.5	2.5	-1.5	1.5
Propagation delay from DCLK to DHS	1.0	4.5	0.5	3.5	-0.5	2.5	-1.5	1.5
Propagation delay from DCLK to DVS	0.5	4.5	0.0	3.5	-1.0	2.5	-2.0	1.5
Propagation delay from DCLK to DEN	1.0	4.5	0.5	3.5	-0.5	2.5	-1.5	1.5
Propagation delay from DCLK to DOVL	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Note: DCLK Clock Adjustments are the amount of additional delay that can be inserted in the DCLK path, in order to reduce the propagation delay between DCLK and its related signals.

Table 23. 2-Wire Host I/F Port Timing

Parameter	Symbol	MIN	TYP	MAX	Units
SCL HIGH time	T_{SHI}	1.25			us
SCL LOW time	T_{SLO}	1.25			us
SDA to SCL Setup	T_{SDIS}	30			ns
SDA from SCL Hold	T_{SDIH}	20			ns
Propagation delay from SCL to SDA	T_{SDO3}	10		150	ns

The above table assumes OCM_CLK = R_CLK / 2 = 100 MHz (default) (ie 10ns / clock)

Table 24. 6-Wire Host I/F Port Timing

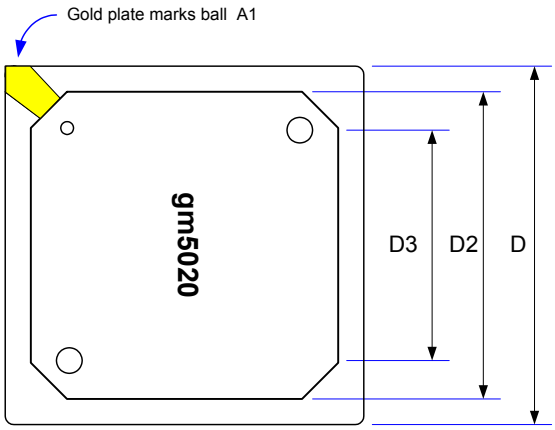
Parameter	Symbol	MIN	TYP	MAX	Units
HCLK HIGH time	T_{SHI}	100	-	-	ns
HCLK LOW time	T_{SLO}	100	-	-	ns
HFSn to HCLK Setup	T_{SDIS}	30	-	-	ns
HFSn from HCLK Hold	T_{SDIH}	20	-	-	ns
HDATA to HCLK Setup		30	-	-	ns
HDATA from HCLK Hold		20	-	-	ns
Propagation delay from HCLK to HDATA	T_{SDO3}	10	-	100	ns

The above table assumes OCM_CLK = R_CLK / 2 = 100 MHz (default)

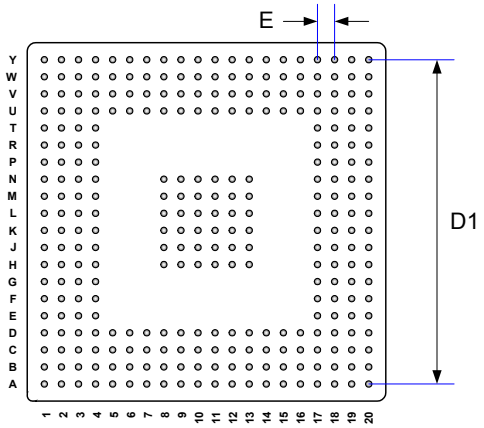
6. ORDERING INFORMATION

Order Code	Application	Package	Temperature Range
gm5020	SXGA	292-pin PBGA	0-70°C
gm5020-H	SXGA with HDCP	292-pin PBGA	0-70°C

7. MECHANICAL SPECIFICATIONS



Symbol	mm			inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.20	2.33	2.46	0.087	0.092	0.098
A1	0.50	0.60	0.70	-	0.024	-
A2		1.17			0.046	
B	0.60	0.75	0.90	-	0.030	-
C		0.56			0.022	
D	26.80	27.00	27.20	1.055	1.063	1.071
D1	-	24.13	-	-	0.950	-
D2		24.00			0.945	
D3		16			0.63	
E	-	1.27	-	-	0.050	-
F	-	-	0.15	-	-	0.006
G		30^0			30^0	



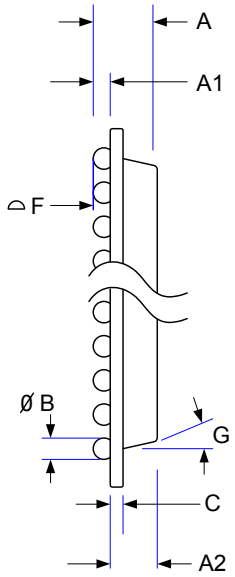


Figure 63. gm5020 292-pin PBGA